

# COMPUWARE

肯微科技股份有限公司

## Release Document

Document Name
<b>Product Specification</b>

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Component P/N		Page	43

### History Record

Date	Description	Revision
2011-11-15	Release	0
2012-03-06	Revise lout 10% load and lin 20% load accuracy on page44	1

Approved By	Signing By	Prepared By
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## 1. Introduction

This document contains technical specification for 1.4KW 1U AC-DC power supply. It's based on current gold level efficiency 1400W PWS-1K41F-1R in 1U share same case housing. Also this power is Digital PFC solution with 80+ certified platinum efficiency; highest efficiency 94.5%+. The power supply will accept a wide input voltage range of 90 to 264Vac, while providing precisely regulated 12Vdc output voltage of 1.2KW at 115Vac and 1400W at 230Vac. The power supply will encompass all protective features and conform to safety agency regulatory requirements. The power will be designed for redundant operation and includes an active Or'ing circuit for isolation. I2C circuit and PMBus protocol will be included to interface with external devices for communication.

Turn on or off the power supply output, either through the hardware control line or the PMBus OPERATION command. Monitor real-time data. Items such as input voltage, output voltage, output current, temperature, and warnings/faults are continuously monitored and displayed. Configure the control law accelerator (CLA) coefficients through an interactive design tool Configure common operating characteristics such as Vout, warning and fault thresholds, and switching frequency. Emerging alternative energy technologies for energy production, control, transmission, and storage

## 2. Technical documentation deliverables

1. Design verification Test Report. –
2. Qualification Report
3. Manufacturing Qualification Report
4. Safety Agency Compliance
5. Component Stress Analysis – This should include measurements on power train critical components against CW design margins. Should include turn on and off measurements (waveforms where applicable) at full and light load and at temperature (-5, ambient and 50°C) where applicable. Please refer to the embedded document for further details



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6. Temperature Output - Input == 5°C
7. Reliability Verification Report – Refer to section 12.7
8. Engineering Samples with technical datasheet
9. Manufacturing/quality Audit
10. Production Schedule

### 3. Electrical specification

Table 1 Input voltage specification

Characteristics	Conditions	Min	Typ	Max	Units
Input voltage range		90	120/240	264	V <sub>ac</sub>
Input current	Full load @ 100VAC			15	A
Input Frequency		47	50/60	63	Hz
Input voltage power-on	Must have a minimum 2V of hysteresis between off	81		89	V <sub>ac</sub>
Input voltage power-off	Must have minimum 2V of hysteresis between on	79		87	V <sub>ac</sub>
Inrush current	First half cycle			25	A <sub>pk</sub>
Input over current protection	In-line fuse			20	A
Power Factor Correction	All specified input AC voltage; Full load/ >25% load		≥0.9/ ≥0.75		

Table 2 Output Voltage specification

Characteristics	Conditions	Min	Typ	Max	Units
Output voltage set point	Nominal line@full load	11.95	12	12.05	V <sub>dc</sub>
Output Power	@230Vac			1400	W
Output Power	@115Vac	1200			W
Output current		1		117	A
Line/Load Regulation		11.52		12.6	V
Standby Voltage 5.0V set point		4.95	5.0	5.05	V
Standby current		0		6	A
Standby line/load reg		4.8		5.25	V
Ripple & noise 12V <sub>out</sub> 5V <sub>Standby</sub>	V <sub>in</sub> = 90-264V <sub>ac</sub> ; Full load; 20MHz Bandwidth; Co = 0.1μF ceramic + 10μF tantalum			120 50	mV mV
Transient Response	12V <sub>o</sub> →50% max step load@ 0.5A/μs, 2200μF capacitive load 5V <sub>sb</sub> →25% max step load @0.5A/μs, 1μF cap load	11.52 4.8		12.6 5.25	V V
Efficiency	V <sub>in</sub> = 100-240vac; 50% - 100% of load; At 20% load	91 90		94.5	% % %

Table 3 Protection Characteristics

Characteristics	Conditions	Min	Typ	Max	Units
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Output current limit 12V 5Vsb		130 7		160 9	A A
Output short-circuit current	Resistance 0.1 ohm or less	Latch-off			
Over voltage protection 5V standby				14.5 6	V <sub>dc</sub> V <sub>dc</sub>
Output under voltage limit		10.5			V <sub>dc</sub>
Over temperature protection	Based on temperature limiting component		TBD		°C

**Table 4 Feature Characteristics**

Characteristics	Conditions	Min	Typ	Max	Units
AC on Delay	V <sub>in</sub> → output regulation range			2500	ms
Hold up time	V <sub>in</sub> =90 – 264Vac; full load	17			ms
Active Load share Accuracy	Compensation for positive rail only; For +25% to 100% full load current			±10	%I <sub>o, rated</sub>
Capacitive load 12V 5Vsb		1K 100		40K 1K	μF μF
On/off# Output enable (on) Output disable (off)	Signal pulled low Signal pulled high (open)	2.0		0.8	V V
DC good signal	Open collector DC Good → signal pulled high that delayed from +12V regulation	100		110	ms
LED DC good LED AC/5Vsb good LED	Green color Amber color				

## 4. AC Requirements

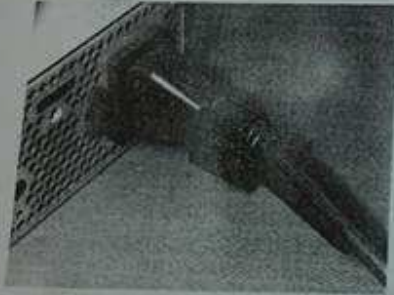
### 4.1 AC Input

Add cable clamp on PS chassis:

電線固定座 WIRE MOUNT

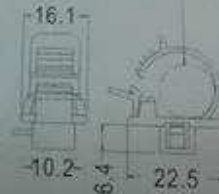
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- ◆ FLAME CLASS :94V-2
- ◆ COLOR:BLACK
- ◆ UNIT:mm

●用途



CHASSIS Ø4.8  
THICKNESS 0.8~2.0

CLOSE Ø13~Ø11



SWPL-1A  
CABLE CLAMP



SWPL-1B  
CABLE TIES

PART NO	PACKAGE
SWPL-1	100

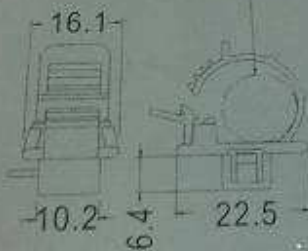


落，造成電腦停機。

IS Ø4.8  
ESS 0.8~2.0

CHASSIS Ø4.8  
THICKNESS 2.0~3.0

CLOSE Ø13~Ø11



SWPL-1A  
CABLE CLAMP



SWPL-2B  
CABLE TIES

PART NO	PACKAGE
SWPL-2	100

The power supply shall operate over wide input voltage range and line frequency described in input specification table.

The power supply must operate within all specified limits over the following input voltage range. Harmonic distortion of up to 10% THD must not cause the power supply to go out of the specified limits. 5% is our target at full load and 10% at 20% load with 230VAC input. The power supply shall operate properly at 87 VAC input voltage to guarantee proper design margins.

#### **4.2 AC Input Connector**

The AC input connection shall be accomplished in combination with DC output connector (FCI P/N 51720-0601603AB). The AC section of the inlet is rated for 15A/250Vac or greater than 14A. Refer to the power supply mechanical drawing for the physical location of the AC input/DC output connector.

#### **4.3 Harmonic Current**

This power supply shall meet latest EN61000-3-2/-3 requirement for ITE instrument. When measured at full output load and 50% of full output load.

#### **4.4 Input under/over voltage protection**

The power supply shall shutdown when the input voltage is under or over the shutdown threshold limits (268 to 275Vac). The power supply shall recover automatically when the input voltage is restored to normal operation limits. There shall be sufficient hysteresis build in circuit to ensure no oscillation is observed. The power supply shall issue noted alarms to provide status until input AC voltage is completely removed.

#### **4.5 AC Inrush Current**

After AC power is applied to the power supply, any initial inrush current surge or spike of 10 milliseconds or less shall not exceed 40 amps peak. Any additional inrush current surges or spikes in the form of AC cycles or multiple AC cycles greater than 10 milliseconds and less than 150 milliseconds shall not exceed 25 amps peak. All internal components (including the fuse, bulk rectifiers and surge limiting device) must be able to withstand the surge current without damage, the peak inrush current shall be less than the ratings of its critical components for all conditions of line voltage, as defined in "AC Input", and during the power line disturbances specified in section "**Power Line Disturbance Requirements**". Repetitive On/Off cycling of the AC mains shall not damage the power supply. The inrush current limit impedance shall be bypassed by either a relay contact or other low impedance device during normal operation.

#### **4.6 Power Factor Correction**

The power supply must exhibit a power factor equal to or better than 0.95 at any input mains voltage and measured at full rated load. For any load less than maximum, the apparent power shall never exceed the maximum load apparent power. Furthermore, for any load greater than 25% of maximum (as described in DC Load Requirement) the power factor must be at least 0.9.

#### **4.7 AC line isolation**

The primary and secondary circuit shall be electrically isolated from each other and from the case. The power supply shall meet all safety agency requirements for dielectric strength including reinforced insulation per standard UL60950 and IEC60950.

## 5. Output Requirements

### 5.1 DC output voltage

The power shall be designed to provide precisely regulated single output as defined in specification table.

+12V output voltages must lower than 0.05V when stay with 5Vsb.

### 5.2 DC output power

The power supply shall be capable of delivering full 1.2KWatts at the 115Vac input voltage and 1.6KWatts at the 230Vac input voltage.

### 5.3 DC output regulation

The power supply shall comply with regulation limits listed in specification table. Regulation shall be measured at the termination points of the remote sense leads. This limit shall be maintained under following list of conditions.

- Input AC line voltage changes due to steady state variation from minimum to maximum as specified in **AC Input**.
- Input line voltage transients.
- Load changes as defined in specification table.
- Interactions between outputs as a function of their loads (including dynamic and static loads).
- Ripple voltage as defined in section “**output ripple & noise**”.
- Component changes due to manufacturing tolerances
- Component changes due to aging.
- Component changes due to self-heating (warm-up drift)
- Environmental changes within the bounds specified for ambient temperature, altitude, airflow and vibration.
- The step load may be applied to any static combination defined in Sections “**output transient response**”.

### 5.4 Output Remote sense

The 12V output shall have provision for remote voltage sense. With the remote sense connected to the assigned voltage wire, the regulation limits specified in the specification table applies. The remote sensing must be able to compensate for a maximum voltage drop of 300 mV on the positive voltage distribution rail. When the remote sense wires are disconnected from the remote sense point, a default sensing location will be the output connector the power supply.

### 5.5 Output ripple & noise

The power supply shall comply with the specified limits over the entire range of operating conditions. The output voltage ripple shall be measured at the pins of the mating output connector. Ripple is defined as an AC differential voltage between the output voltage pins and return pins, that is present on the power supply output. This definition includes, but is not restricted to, AC voltage that is due to line voltage ripple, switching frequency ripple and dynamic loading. For the purpose of this measurement, the remote sense wires will be tied the output voltages directly at the pins of the mating output connector. Ripple voltage shall be measured with a 0.1uF ceramic capacitor in parallel with a 10uF electrolytic capacitor connected between the measured voltage and its return. Conformance to this requirement shall be measured using a differential amplifier with 20 MHz bandwidth.

### 5.6 DC Common to Frame Connection

DC common shall be connected to frame ground in the power supply.

### 5.7 Output transient response

The power supply shall maintain compliance to the specified limits during a dynamic load condition. The output shall remain within the specified limits for the step loading and within the limits specified in below table. The load transient repetition rate shall be tested between 50 Hz and 5 KHz at duty cycles ranging from 10% - 90%. The step load may occur anywhere within the min load to the max load, but the peak load will not be over 25% of max load.

Transient load requirements

Output	Step load size	Load slew rate	Capacitive load
12V	50% of max load	0.5A/us	3000uF
5Vsb	25% of max load	0.5A/us	1uF

### 5.8 Efficiency

The power supply efficiency (watts output/watts input) shall be equal to or greater than 94.5%+ at the 50% of maximum load defined in platinum Level specification table with 100VAC to 240VAC input AC range. Also we required greater than 94%+ efficiency with 1.4KW loading at 230VAC.

### 5.9 Stability

The power supply shall maintain stable operation over all conditions listed below. The phase margin must be a minimum of 45° where the gain is less then or equal to 1.

- DC and dynamic loads as defined in their respective sections.
- All input conditions as defined in section "**AC Input**"
- All environmental conditions as defined in section "**Environmental Requirements**"
- All load capacitance ranges as defined in section "**Load Capacitance**"
- The power supply must also be stable when powering a negative impedance load such as Voltage Regulation Module (VRM).
- The gain and phase plots using actual VRM and hard disk drive loads have to be taken and should meet 45 degree phase margin requirement.

### 5.10 Output voltage overshoot at start up and shutdown

During start up, the output voltage shall rise monotonically to within 5% of Vo, rated and must be in regulation band within 13 ms. During shutdown, the output voltage shall be within 5% of rated output and decay monotonically to ground level. There shall be no positive excursion during shutdown.

### 5.11 Output No Load Operation

If the load is removed from the output, the following must be maintained:

- No internal component stressed beyond its rating.
- The supply must start up and operate.

This condition shall cause no damage to the power supply. Protection circuits must not disable the power supply. The power supply shall operate with no load on all DC outputs. Output regulation may be relaxed to +/-20% during this condition, however **DC GOOD signal must stay high**. Protection circuits must not be disabled in this mode of operation.

### 5.12 Residual Voltage

The residual voltage at 12V output for no load condition shall not exceed 100mV when AC voltage is applied to the supply under DC "OFF" condition.

### 5.13 Output Repetitive Step Load

The output shall withstand a peak step load defined by the following conditions:

- 1) The summation of the average value of the step load and the static load shall not exceed 100A.
- 2) Step peak amplitude shall not exceed 125A.

### 5.14 Output Reverse EMF

The power supply shall be able to start even if there is a **Reverse EMF** of up to 3V on +12V output:

- 1) After initial startup.
- 2) After the power supply is turned off using either the "On/Off#" signal.
- 3) After removing AC power and then reapplying.

### 5.15 Load Capacitance

For stability and power up considerations, the maximum and minimum load capacitance is as follows

Load Capacitance		
Voltage	Minimum capacitance	Maximum capacitance
+12V	1000 $\mu$ F	40,000 $\mu$ F
+5Vsb	100 $\mu$ F	1,000 $\mu$ F

### 5.16 Power Leakage

Any combination in one system with 1 to 4 redundant power supplies; leakage current is less than 3.5mA for total. Output +12V and PWOK even power connect to PDB with +5V, +3.3V, -12V must less than 50mV when 5Vsb before power turn on.

## 6. Protection Requirement

### 6.1 Primary Protection

The supply must have internal primary over-current protection. A normal blow fuse must be placed in the line side of the input circuit. The input power line must be fused in accordance with the safety requirements of section "**Safety**". The input fuse must be rated at 20A or less. This fuse is not to be considered replaceable for purposes of determining power supply reliability and operating life as specified in section.

If any component on the line side of the fuse is shorted or opened, it may not cause a fire or any other safety risk. The fuse must be approved by UL, TUV. The PC board must be labeled "Replaced only with (YYYYYY) P/N XXXXXX".

YYYYYY= Fuse Vendor Name XXXXXX=Fuse Vendor Part Number

### 6.2 Secondary Protection

#### 6.2.1 Shutdown Definition

Shutdown is defined as a condition where the 12V output latches off. 5Vsb shall remain on. The shutdown latch shall be reset by either removal of the AC input power or changing the "**On/Off#**" signal state. The power supply shall not latch off because of under voltage condition on the output unless it is caused by an overload condition.

### **6.2.2 Output over current protection**

The power supply shall include current limit circuit to provide protection against over load condition. In an event of output current exceeds the over current limit threshold defined in specification table, the output will latch-off and remain off. The output shall be recovered per shutdown definition. During such event, the standby must remain ON unless the fault is cause by standby over load condition. For standby overload condition, current fold back method is preferred. The standby output should not latch off. The standby must return to normal operation once the fault is removed.

Notes:

- 1) Over current on the output must not trip due to dynamic characteristics of the +12V load, as defined in transient response section.
- 2) The power supply shall shut down when an applied 10A per second ramp reaches the maximum continuous current trip point.

### **6.2.3 Short circuit protection**

The power supply shall latch off and suffer no physical damage when the output is shorted to its DC return, however 5Vsb should continue to operate normally under this condition. The power supply shall not latch off if 5Vsb signal shorts to its DC return. A short circuit is considered to be resistance of 0.1 Ohms or less.

### **6.2.4 Output over voltage protection**

The power supply shall include an independent protection circuit that provides protection in an event of over voltage condition at the output connector.

In an event of over voltage condition, the power supply must shutdown and latch off. 5Vsb must continue to operate normally.

Over voltage protection circuits shall not cause the power supply to shutdown as long as the output voltages are within regulation limits.

The protection circuitry must be independent from the regulation circuitry including voltage references and secondary-primary feedback elements.

No single component failure may cause a sustained over voltage.

**Note:** A shutdown caused by an over voltage in one power supply will not cause the other power supply in parallel to shutdown.

### **6.2.5 Output under voltage protection**

The power supply shall not latch off due to Under-Voltage condition on any one of the outputs unless it is caused by an overload condition on the output. Under voltage circuits shall not cause the supply to shutdown as long as the output voltages are within regulation limits. The protection circuitry must be independent from the regulation circuitry, including voltage references and secondary-primary feedback elements.

### **6.2.6 Over temperature protection**

A temperature sensing device, or devices, internal to the power supply shall monitor critical component(s) temperature(s). If monitored component(s) critical temperature(s) is (are) reached, the power supply shall stay in regulation for 30 seconds then latch off all outputs except +5Vsb. The critical temperature is to be determined (TBD).

## 7. Power Supply Sequencing

Power supply output voltages timing shall follow signal requirement section of this document and 13.11 of SSI ERP2U power supply design guide, V2.0, except for 5V, 3.3V, and -12V (See Below).

### 6.11 Timing Requirements

STATUS
Required

These are the timing requirements for the power assembly operation. The output voltages must rise from 10% to within regulation limits ( $T_{vout\_rise}$ ) within 5 to 1:3: ms. The +3.3 V, +5 V and +12 V output voltages should start to rise at about the same time. All outputs must rise monotonically. The +5 V output needs to be greater than the +3.3 V output during any point of the voltage rise. The +5V output must never be greater than the +3.3V output by more than 2.25 V. Each output voltage shall reach regulation within 50 ms ( $T_{vout\_on}$ ) of each other during turn on of the power supply. Each output voltage shall fall out of regulation within 400 ms ( $T_{vout\_off}$ ) of each other during turn off. Figure 2 and Figure 3 show the turn ON and turn OFF timing requirements. In Figure 3, the timing is shown with both AC and PSON# controlling the ON/OFF of the power supply.

Table 24: Output Voltage Timing

Item	Description	MIN	MAX	Units
$T_{vout\_rise}$	Output voltage rise time from each main output.	5	1:3:	ms
$T_{vout\_on}$	All main outputs must be within regulation of each other within this time.		1:3:	ms
$T_{vout\_off}$	All main outputs must leave regulation within this time.		400	ms

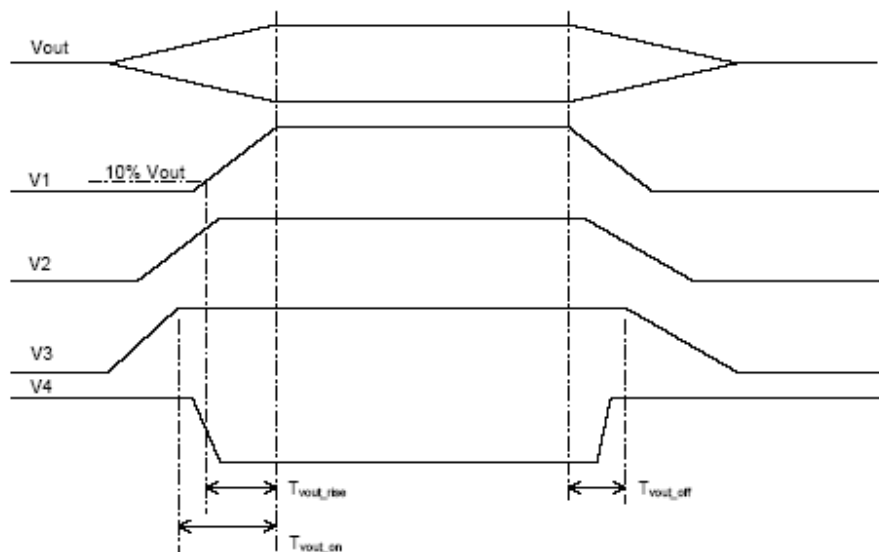
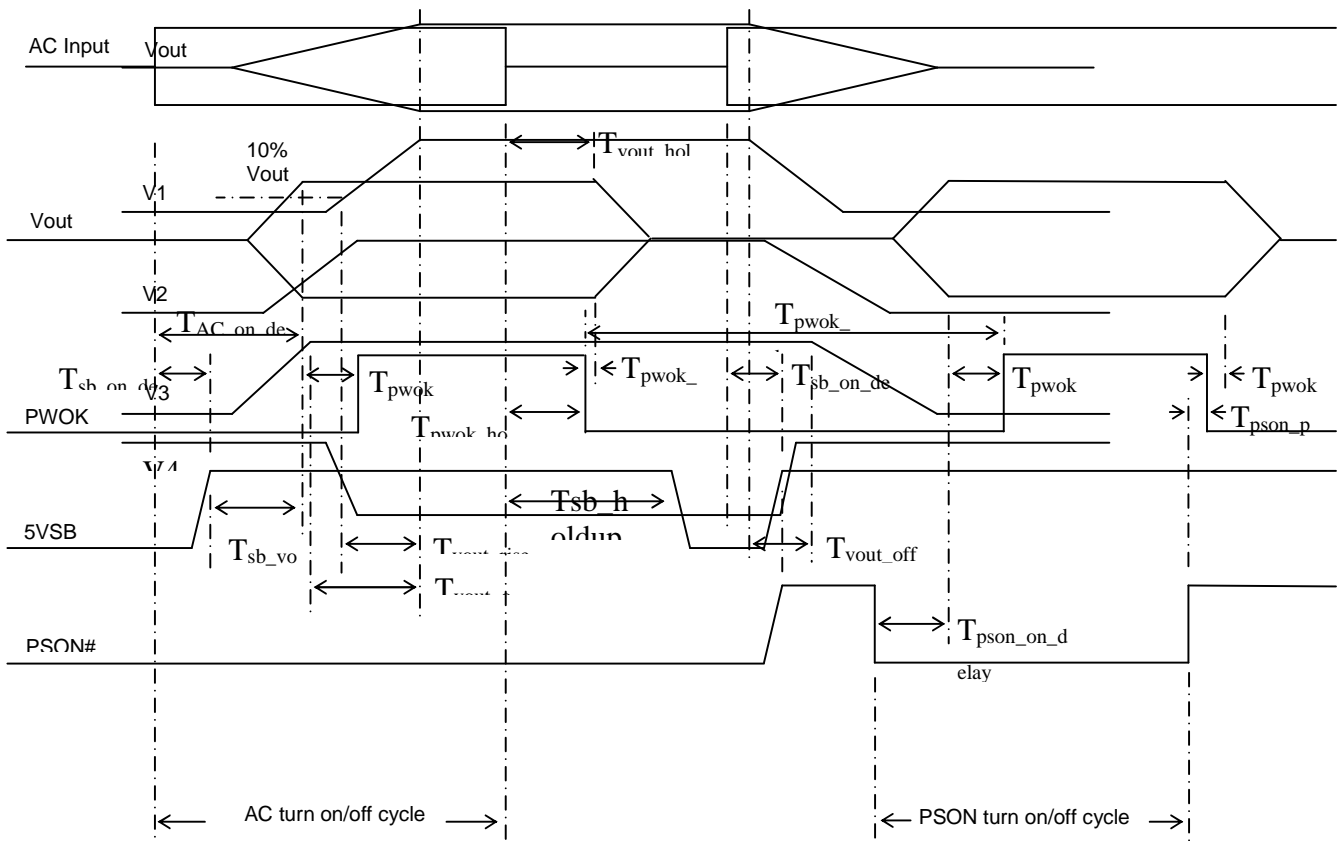


Figure 2: Output Voltage Timing

## Timing Requirements

Figure 2 Turn On/Off Timing (Signal Power Supply)



Item	Description	MIN	MAX	Units
Tsb_on_delay	Delay from AC being applied to 5 VSB being within regulation.		1500	ms
T ac_on_delay	Delay from AC being applied to all output voltages being within regulation.		2500	ms
Tvout_holdup	Time all output voltages stay within regulation after loss of AC at 75% load	17		ms
Tdc_good_holdup	Delay from loss of AC to deassertion of DC Good	16		ms
Tpson_on_delay	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
Tpson_dc_good	Delay from PSON# deactive to DC Good being deasserted.		50	ms
Tdc_good_on	Delay from output voltages within regulation limits to DC Good asserted at turn on.	100	110	ms
Tdc_good_off	Delay from DC Good deasserted to output voltages dropping out of regulation limits.	1		ms
Tdc_good_low	Duration of DC Good being in the deasserted state during an off/on cycle using AC or the PSON# signal.	100		ms
Tsb_vout	Delay from 5 VSB being in regulation to O/Ps being in regulation at AC turn on.	50	1000	ms
Tsb_holdup	Time 5VSB output voltage stays within regulation after loss of AC.	70		ms
Tsb_Vout_rise	The rising time for +5VSB start up to be in regulation	1	25	ms
T12_Vut_rise	The rising time for +12V start up to be in regulation or rising slope 1V/ms	5	12	ms

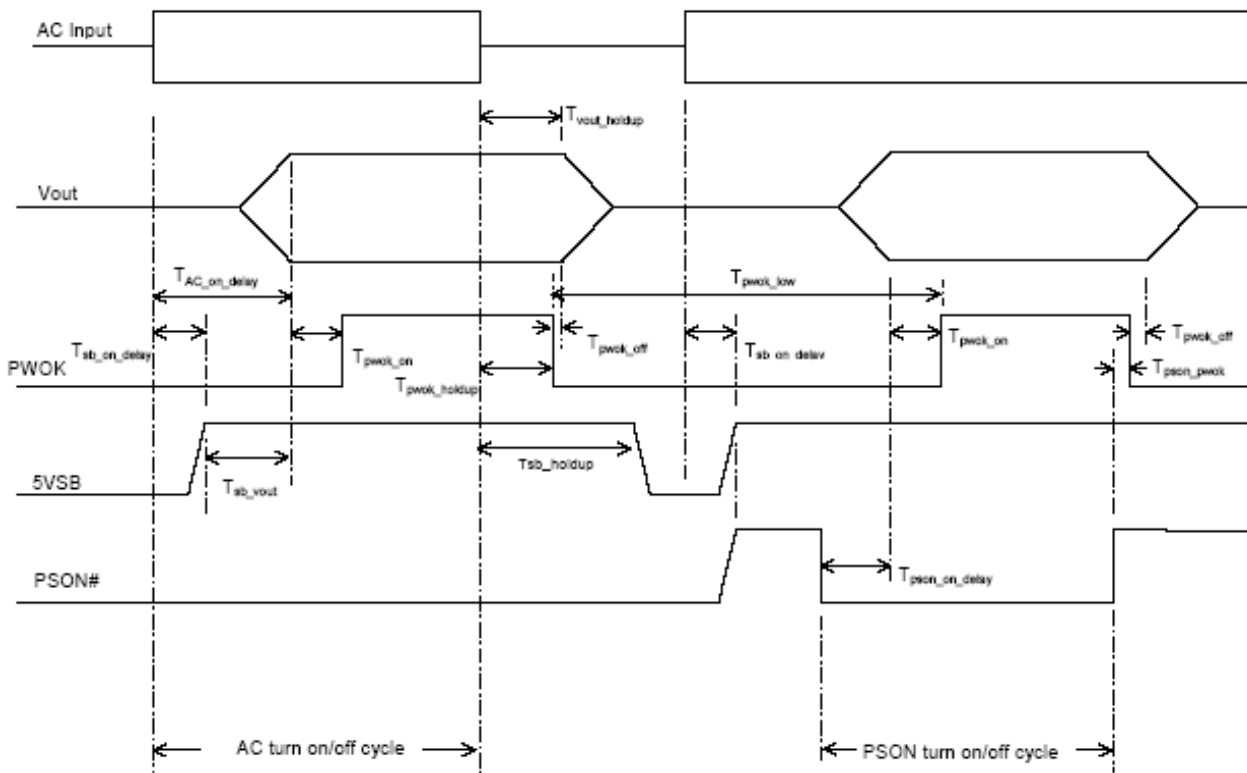


Figure 3: Turn On/Off Timing

### 7.1 Output sequencing

The power supply shall be turned-on by one of two ways:

With AC already applied, by driving the "On/off#" input signal to a low state. When the "On/off#" signal is transitioned to LOW state, the output must be in regulation within 400 ms maximum and the LED shall be lit with green color if the power supply is operating normally. By applying AC to the primary input, with the "On/off#" input signal tied to a low state. With this method, the output must be in regulation within 2500ms and the LED shall be lit with green color if the power supply is operating normally.

When AC power is applied to the power supply, LED on the front panel of the power supply shall be illuminated with amber color.

### 7.2 Standby Sequencing

5Vsb shall be on (high) whenever AC Voltage is within the input range specified in "AC Input".

### 7.3 Auto Restart

The power supply shall be capable of automatically restarting due to a temporary AC outage. When AC returns, it is assumed to be within the operating range defined in section "AC Input".

### 7.4 Reset After Shutdown

When the power supply latches into shutdown either due to an internal power limit condition or due to a fault on an output (over current or short circuit), it shall return to normal operation only after the fault has been removed and the power supply is reset. Reset can be accomplished in one of two ways:

By toggling the “**ON/OFF#**” signal from low-to-high-to-low. The duration of the 1st low time necessary to reset the power supply must be no longer than 100 msec.

By removing primary power. AC must be removed for at least one second before reapplying.

### 7.5 Power Supply Behavior When Faulted

A faulted power supply shall not sink more than 100 ma current from the 12V output. The I2C bus status shall be operational and valid.

A power supply that fails due to an Over-Voltage condition will shutdown gracefully and will not cause shutdown of other power supplies in parallel. Standby supply will remain on.

## 8. Controls and Monitoring

### 8.1 Signal Requirements

All output logic signals will be open collector and 5V compatible except I2C signals (clock and data) which are 3.3V compatible. The power supply will sink less than 1uA as a logic high and sink at least 20 mA as a logic low. A logic low must be less than 0.4V while sinking 20mA. Signal transitions, with a 10K Ohm resistor pulling the output to 3.3/5.0V, must be clean (glitch free) and bounce free. The rise/fall time can be no slower than 5usec, measured at 10% and 90% points. The power supply will pull each logic input up to 3.3V with a resistor whose value is between 10K Ohm and 50K Ohm and provide a 100pF ceramic capacitor, signal to ground. The power supply will accept 0.8V or less as a logic low and 2V or greater as a logic high. There will be a 300mV, minimum hysteresis between a logic low and a logic high. The host will be able to sink 0.5 mA for a logic low. I2C clock and data signal shall meet 3.3V logic high and low. I2C clock and data signal line shall not add capacitor. I2C clock bus frequency is about 10 KHz, and signal rise/fall time at 5µs to 300ns shall not affect I2C functions.

### 8.2 Direct Signals

These signals are wired directly from the power supply to the system, which are shown on pin assignment diagram.

### 8.3 On/Off#

The **ON/OFF#** signal is an active low input used to activate the power supply 12 output voltage. If AC input is already applied, the 12V output shall be within regulation no less than 100ms after **ON/OFF#** is pulled low. When this signal is HIGH the power supply must remain off.

### 8.4 DC Good

The power supply shall provide an output signal, “**DC GOOD**”, which indicates that the 12V output is within the OV/UV limits.

**Note:** The “**DC GOOD**” signal shall be terminated at near of the output power supply connector with a 0.01 uF ceramic capacitor to filter out unwanted noise voltage.

**DC GOOD (high +12V and low 0V)** Delay from PSON# deactive to DC GOOD being deasserted max 50ms. Delay from loss of AC to deassertion of DC GOOD. Tested at 75% of maximum load and over 100-240VAC input **minimum 19ms.**

*Table 4: PWOK Signal Characteristics*

<b>Signal Type</b>	+12V TTL Compatible output signal	
<b>PWOK = High (+12V)</b>	Power DC GOOD	
<b>PWOK = Low (0V)</b>	Power DC not GOOD	
	MIN	MAX
Open collector DC Good → signal pulled high that delayed from +12V regulation	100ms	110ms

#### 8.4.1 Status during Over-temperature

When the power supply maximum temperature is exceeded, the “**DC GOOD**” signal must go LOW at least 5ms before 12.2V output is removed.

#### 8.4.2 Status during DC Turnoff and AC Outage

When the **ON/OFF#** signal is cycled HIGH, the “**DC GOOD**” signal shall go LOW a minimum of 1 ms prior to 12V dropping out of regulation as described in section “**DC output regulation**”. DC GOOD signal shall remain HIGH for at least 17 ms after AC power is removed and shall go LOW at least 1 ms before any output voltage falls below the regulation limits described in “**DC Output regulation**”.

#### 8.4.3 Status during PLD

DC GOOD signal shall remain HIGH during the “error free” part of Power Line Disturbances (PLDs) defined in section “**Power Line Disturbances (PLD) Requirements**”.

#### 8.5 Present Detect#

The “**Present Detect#**” signal shall be pulled HIGH by the system. This signal pin is hard wired to ground in the power supply and alerts the system whenever a power supply is inserted into the slot.

#### 8.6 Ishare

This is an analog signal that is used to insure current sharing of the 12V output between two power supplies. It also represents the amount of the loading on the power supply (or supplies). It is noted that, with two power supplies sharing current, the percentage is the combined current for two power supplies, not one. The Host system may use this signal to monitor power supply loading.

Ishare Voltage	
% of max. current capacity	Voltage level (+/- 10%)
25%	2V
50%	4V
100%	8V

#### 8.7 Remote Voltage Sense (+ & -)

The remote voltage sense signal is used to keep the 12V output voltage within regulation at load. In an event of the sense line is shorted to DC return, 12V output shall be latch off.

## 9. Standby Voltage requirement

### 9.1 Standby output voltage diode/FET Or'ing

The power supply shall have ORing diode/FET that allows the 5Vsb to be connected in parallel with another 5Vsb power supply. If an internal fault occurs on the primary circuits, the internal logic of the power supply I2C will continue to operate from the OR'ed 5Vsb of the unit operating in parallel.

### 9.2 Standby Current Sharing

5Vsb is not required to share current.

### 9.3 Standby supply stability

5Vsb shall be unconditionally stable under all system load and AC line conditions while operating alone or in parallel with one or more power supplies.

### 9.4 Standby Over voltage Protection

The power supply will shut down if 5Vsb on the anode side, exceeds 6V plus the ORing diode voltage drop. The protection circuitry must be independent from the regulation circuitry including voltage references and secondary-primary feedback elements. No single component failure may cause a sustained over voltage.

**Note:** A shutdown caused by an over voltage in one power supply will not cause the other power supply in parallel to shutdown.

### 9.5 Standby Current Limit Protection

The 5Vsb current limit threshold is defined in specification table. Refer to section "Output over current protection" for detailed description.

## 10. Redundancy/ N+N Operation

### 10.1 Current Sharing Operation

The power supply shall be designed for active current sharing.

Two power supplies will be paralleled in a system. Each power supply must be able to share load to within +/- 10% share error measured 25, 50, 100% of single power supply full load current.

**5Vsb requires an "ORing" diode to provide protection against internal short circuit fault.**

### 10.2 Output Isolation Oring MOSFET

The 12V output current must pass through an Oring MOSFET to protect the bus voltage against a power supply internal fault.

### 10.3 Power Supply Behavior When Faulted

- The faulted supply shall not sink more than 100 ma current.
- I2C bus status shall be operational and valid, refer to "**I2C Bus/VPD Interface**".
- The "DC Good" signal and "DC Good Fault" bit status shall be valid.
- A power supply that fails due to a 12V or 5Vsb Over-Voltage condition will shutdown gracefully and will not cause shutdown of the other power supplies in parallel.

### 10.4 Parallel operation stability

The power supply shall exhibit stable operation under no/full load, full input voltage range and overall operating temperature conditions when operated in parallel.

## **10.5 Hot Swap Operation**

The power supply must be designed with “hot swap” function with or without active AC line cord. After Hot swap I2C address shall be same as host power supply backplane hardware assigned. Host existing working power supply shall not be affected by hot swapping power supply.

## **11. Light Emitting Diodes (LED)**

All LEDs shall protrude beyond the supply chassis surface for improved visibility. A single 2 color (green/amber) LED will be used in this power supply.

### **11.1 DC Good LED Indicator**

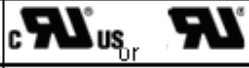
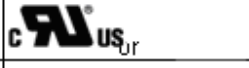


A green/amber double color Light Emitting Diode (LED) shall be mounted as indicated in mechanical drawing and shall indicate the status of the DC GOOD signal with green color. The LED shall continue to glow under normal operation of the power supply. If this LED is not lit the power supply is **not** operating properly.

### **11.2 AC/5Vsb Good LED Indicator**

The green/amber Light Emitting Diode (LED) shall be mounted as indicated in mechanical drawing and shall indicate the status of the 5Vsb within regulation range, 12V is off and the AC line voltage is within the operating range of the power supply. The LED will show a status of amber under this condition.

## 12. Power Supply Compliance Agency and Environmental Requirements

### 12.1 Safety and EMI

Regulatory Certification/Compliance Plan			
Item	Certification	Required Country	Acceptable Markings
1	Product Safety Compliance/Certification		
1.1	UL60950	US	
1.2		Canada	
1.3	EN60950	Europe	
1.4	IEC60950 and National Deviations	International	none
1.5			none
1.6			none
1.7	Bauart Marking	Germany	
1.8	CE Marking: Low Voltage Directive 73/23/EEE	Europe	none
1.9	GB4943- CNCA Certification ("GB=Guo Biao", means "National Standard").	China	
1.10	BSMI – Safety Certification (Safety, EMC)	Taiwan	none
1.11	CB Reporting with applicable deviations	Nation als	none
2	Product EMC Compliance/Certification		
2.1	FCC part 15	USA	none
2.2	ICES-003 - Emissions	Canada	none
2.3	CISPR 22 – Emissions	International	none
2.4	EN55022 - Emissions	Europe	none
2.5	EN61000-3-2 - Harmonics	Europe	none
2.6	EN61000-3-3 - Voltage Flicker	Europe	none
2.7	CE – EMC Directive 89/336/EEC	Europe	none
2.8			none
2.9			none
2.10	BSMI CNS13438 Emissions	Taiwan	none
2.11	GB 9254 – (EMC) Certification	China	none
2.12	GB 17625 - (Harmonics) CNCA Certification	China	none
2.13	EN55024 - Immunity (Europe)**		
	a) EN61000-4-2 Electrostatic Discharge	Europe	none
	b) EN61000-4-3 Radiated RFI Immunity	Europe	none
	c) EN61000-4-4 Electrical Fast Transients	Europe	none
	d) EN61000-4-5 Electrical Surge	Europe	none
	e) EN61000-4-6 RF Conducted	Europe	none
	f) EN61000-4-8 Power Frequency Magnetic Fields	Europe	none
	g) EN61000-4-11 Voltage Dips and Interruptions	Europe	none

**Note: The UUT must be warmed above 30 minutes with max load before run Conducted & Radiated Emission test in lab. The UUT must be verified with 20%, 50%, and 100% of max load (resistor) for main DC-DC output voltage & 5Vsb respectively when run Conducted &**

**Radiated Emission test in lab. Vendor must send Conducted & Radiated Emission testing data of PS to SMC during each developing stage ( DVT, PR and first lot of MP). The power supply itself meets class A with 6dB margin of EMI limits for CE,FCC,CISPR tested with full output resistance loading and certified with CE compliance.**

**12.2 ROHS Compliance**

The unit shall comply with DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment. The 2010 lead exemption will be applicable to this unit.

**12.3 Humidity**

Operating: 20% to 95% RH, Non-condensing.  
 Non-operating:5% to 95% RH, Non-condensing

**12.4 Altitude**

Operating: up to 10,000 feet.  
 Non-operating: up to 35,000 feet

**12.5 Temperature:**

Normal Operating Ambient(at sea level):

0 degrees Celsius minimum (operating and in standby)  
 50 degrees Celsius maximum (operating – power supply on)  
 50 degrees Celsius maximum (standby – AC power only, power supply off)

maximum rate of change is 30 degrees Celsius/hour

Abnormal Operating Ambient(at sea level):

N/A degrees Celsius  
 N/A survival time

**12.6 Power Line Disturbance Requirements**

Unit shall comply with the following requirements;

EU Reference	Title of Standard	International Reference	Test Level Heavy Industrial
EN 61000-4-5	Electromagnetic Compatibility (EMC) – Part 4: -- Section 5: Surge Immunity Test	IEC 1000-4-5	1, 2kV differential 2, 4kV common
EN 61000-4-4	Electromagnetic Compatibility (EMC) – Part 4: -- Section 4: Electrical fast transient/burst immunity test	IEC 1000-4-4	1, 2, 4kV - Power 0.5, 1, and 2kV - Signal

## 12.7 Reliability

The MTBF data shall be presented in couple of methods, 1) a calculation method that will have a minimum MTBF at continuous operation of 100,000 hours at nominal input voltage (110/240Vac), 75% load in an ambient of 35°C, 2) a demonstrated method that will have a minimum of 250,000 hours under similar operating condition. The calculation shall be made in accordance to Bellcore RPP.

## 13. I<sup>2</sup>C and PMBus™ 1.2 standard.

This power support supports both Super Micro I2C function and PMbus. With different addressing, the user should able to use either Super Micro I2C FRU or PMbus commands.

I2C Signal Connector Pin Definition

Pin	Signal	24 AWG Color
1	SMBus Clock	White/Green Stripe
2	SMBus Data	White/Yellow Stripe
3	SMBAlert	Red
4	No connect	
5	No connect	

### 13.1 Super Micro I2C

Slave address will be 0x70 (default), 0x72, 0x74, 0x76

The power supply can be read and written to as if it's an 2k bit (256 byte) I2C EEPROM. The power supply must support: Byte write and Random read. Read and write must work at speeds up to 100 kHz. This bus shall operate at 3.3V but be tolerant of 5V signaling.

All the data stored in the power supply follows FRU spec, IPMI, Platform Management FRU information Storage Definition v1.0.

FRU spec attached below:

17. FRU Information Layout.....	15
18. Record Field Definitions .....	16
18.1 Power Supply Information (Record Type 0x00) .....	16
18.1.1 Overall Capacity in Watts .....	16
18.1.2 Peak VA .....	17
18.1.3 Inrush .....	17
18.1.4 Inrush interval .....	17
18.1.5 Low end Input voltage range 1 .....	17
18.1.6 High end Input voltage range 1 .....	17
18.1.7 Low end Input voltage range 2 .....	17
18.1.8 High end Input voltage range 2 .....	17
18.1.9 Low end input frequency range .....	17
18.1.10 High end input frequency range .....	17
18.1.11 A/C dropout tolerance .....	17
18.1.12 Binary flags .....	17
18.1.12.1 Tachometer pulses per rotation/Predictive fail polarity .....	17
18.1.12.2 Other Binary flags .....	18
18.1.13 Peak Wattage .....	18
18.1.14 Combined Wattage .....	18
18.1.15 Predictive fail tachometer lower threshold .....	18
18.2 DC Output (Record Type 0x01) .....	19
18.2.1 Output Information .....	19
18.2.2 Nominal voltage .....	19
18.2.3 Maximum negative voltage deviation .....	20
18.2.4 Maximum positive voltage deviation .....	20
18.2.5 Ripple and Noise pk-pk, 10Hz to 30MHz .....	20
18.2.6 Minimum current draw .....	20
18.2.7 Maximum current draw .....	20
18.3 DC Load (Record Type 0x02) .....	20
18.3.1 Output Information .....	20
18.3.2 Nominal voltage .....	20
18.3.3 Spec'd minimum voltage .....	20
18.3.4 Spec'd maximum voltage .....	21
18.3.5 Ripple and Noise pk-pk 10Hz to 30MHz .....	21
18.3.6 Minimum current load .....	21
18.3.7 Maximum current load .....	21
18.4 Management Access Record (Record Type 0x03) .....	21
18.4.1 Example .....	22
18.5 Base Compatibility Record .....	24

The “Chassis Info” and “Board Info” are not to be implemented. The “Common Header” and “Product Area” are required.

For the “Multiple Record” area, the power supply should implement the “Power Supply Information”(section 18.1), and multiple “DC Output” section as needed.

For the “Product Info” area must began from offset location 0x18 (offset 0x04 product information offset must contains value of 0x03).

The “Internal Use” section, defined by Supermicro as follows:

Offset		Result of a read
0x09	Temperature	Value to represent the current temperature of the hottest spot inside the power supply This is an unsigned integer value in Celsius.
0x0A	Fan 1 speed (main fan)	Value to represent the RPM of the power supply fan #1  This should be the fan pulse count in 262 ms. We are assuming that two fan pulses equal one rotation.  The system software will convert this value, to fan RPM, using:  $RPM=(1/0.262) * (Fan\ Pulse\ Count * 60 / 2)$
0x0B	Fan 2 speed (secondary fan if available)	Value to represent the RPM of the power supply fan #1  This should be the fan pulse count in 262 ms.

		<p>We are assuming that two fan pulses equal one rotation.</p> <p>The system software will convert this value, to fan RPM, using:</p> $\text{RPM} = (1/0.262) * (\text{Fan Pulse Count} * 60 / 2)$ <p>If fan 2 is not available, default value 0x00</p>
0x0C	Power Status	<p>Value to represent DC GOOD status</p> <p>byte = hex 01 means DC GOOD</p> <p>byte = 00 means no DC output</p>
0x0D	Temperature High Limit	Value is fixed and should be the highest acceptable temperature that the power supply can sustain based on offset 09.
0x0E	Fan 1 speed Low Limit	Value is fixed and should be the lowest fan #1 RPM acceptable
0x0F	Fan 2 speed Low Limit (if secondary fan is available)	Value is fixed and should be the lowest fan #2 RPM acceptable If fan 2 is not available, default value 0x00
0x10	Reserved	
0x11	Reserved	
0x12	Reserved	
0x13	Reserved	
0x14	AC RMS current	This byte, divided by 16, is the AC (RMS) input current.
0x15	DC output current (optional)	This byte is the DC output current. If this function is not available, default value is 0x00
0x16	Firmware version	<p>Example: version 2.0 is encoded as 0x20</p> <p>Anything less than 2.0 (0x20) found at this location will be reported as version 1.0 by Supermicro health monitoring software</p> <p>Default initial value 0x10</p>
0x17	FRU file revision	Integer only
0xF0	AC current limit	AC current upper limit; This byte, divided by 16, is the AC input current limit
0xF1	+12V DC current limit	+12V DC current upper limit; scale factor: this byte is the DC (+12V) output current.
0xF2	Power supply wattage	Power supply wattage; lower byte
0xF3		Power supply wattage; higher byte
0xF4	Input voltage	100-240Vac input voltage reading (for readings above 255Vac, it should report 255Vac)
0xF5	Input power	Real time Input power in watt (lower byte) (example 0x01F4=500W)
0xF6	Input power	Real time Input power in watt (higher byte)
0xFF	Write protection Control	<p>This byte controls whether the FRU is writeable or read only. When this byte content is 0x88, the FRU is writeable. Otherwise, only byte 0xFF can be modified.</p> <p>value= 0x88 is FRU writeable mode</p>

		Any other value, FRU is read only except address 0xFF can be modified. Default value for this byte is read only, 0x00.
--	--	---

The power supply will support the “byte write” procedure defined in the I2C EEPROM spec.

**Read only bytes** --- writes to the following bytes should be ignored:

Offset	
0x09	Temperature
0x0A	Fan 1 speed (main fan)
0x0B	Fan 2 speed (secondary fan if available)
0x0C	Power Status
0x14	AC RMS current
0xF4	Input voltage
0xF5	Real time Input power (lower byte)
0xF6	Real time Input power (higher byte)

**I2C auto-recovery feature:**

In a normal I2C transaction, there will be 8 bytes of transmission plus an ACK (acknowledge) byte, for a total of 9 clock cycles. ACK is done by pulling down the SDA line. If there is a missing clock cycle, the chip doing the ACK will hold down the SDA line indefinitely and hanging the I2C bus. The power supply needs to prevent the above scenario from happening. If the I2C bus SDA or SCL is stuck low for more than 25 ms, the power supply should reset either its I2C communication module, or itself.

The power supply I2C microcontroller should not latch the system I2C bus by pulling SDA or SCL line low for more than 40 ms.

The power supply needs to have 4.7k Ohm internal pull up on the SDA or SCL lines and operate with 3.3V nominal voltage level.

**13.2 PMBus**

The PMbus specification is based on the PMBus specification parts I and II, revision 1.1 and 1.2. PMBus Power System Management Protocol Specification Part I – General Requirements, Transport and Electrical Interface; Revision 1.2; Reference: <http://pmbus.org/specs.html>

PMBus Power System Management Protocol Specification Part II – Command Language; Revision 1.2; Reference: <http://pmbus.org/specs.html>

System Management Bus (SMBus) Specification version 2.0; Reference: <http://smbus.org/specs/>

**13.2.A Addressing**

The power supply PMbus device address locations are shown below. For redundant systems there are up to 2 signals to set the address location of the power supply once it is install in the system: A1, A0. For no-redundant systems the power supply device address location should be 78h.

System addressing Address1/Address0	0/0	0/1	1/0	1/1
Power supply PMBus™ device	78h	7Ah	7Ch	7Eh

Note: Non-redundant power supplies will use the 0/0 address location.

### 13.2.B Hardware

The device in the power supply shall be compatible with both SMBus 2.0 ‘high power’ specification for I<sup>2</sup>C V<sub>dd</sub> based power and drive (for V<sub>dd</sub> = 3.3V). This bus shall operate at 3.3V but be tolerant of 5V signaling.

One pin is the Serial Clock [SCL] (PSM Clock). The second pin is used for Serial Data [SDA] (PSM Data). Both pins are bi-directional, open drain signals, and are used to form a serial bus. The circuits inside the power supply shall derive their power from the standby output.

The PMBus device shall be on whenever AC power is applied to the power supply or a parallel redundant power supply in the system.

1000ns maximum rise time for SDA and SCL

300ns maximum fall time with a 400pF capacitive load for SDA and SCL

10ns minimum fall time with a 20pF capacitive load for SDA and SCL

### 13.2.C Data Speed

The PMBus device in the power supply shall operate at 100khz and avoid using clock stretching that can slow down the bus. For example, the power supply can clock stretch while parsing a command or a power supply servicing multiple internal interrupts or NACK may require some use of clock stretching. Unsupported commands may respond with a NACK but must always set the communication error status bit in STATUS\_CML.

The PMBus device shall support SMBus cumulative clock low extend time (T<sub>low: sext</sub>) if < 25ms. This requires the device to extend the clock time no more than 25ms between START and STOP for any given message.

### 13.2.D Bus Errors

The PMbus device shall support SMBus clock-low timeout (T<sub>timeout</sub>). This capability requires the device to abort any transaction and drop off the bus if it detects the clock being held low for > 25ms, and be able to respond to new transaction 10ms later.

The device must recognize SMBus START and STOP conditions on any clock interval. (These are requirement of the SMBus specifications, but are often missed in first-time hardware designs.) The device must not hang due to ‘runt clocks’, ‘rut data’, or other out-of-spec bus timing. This defined as signals, logic-level glitches, setup or hold times that are shorter than the minimums specified by the SMBus specification. The device is not required to operate normally, but must return to normal operation once ‘in spec’ clock and data timing is again received. Note if the device ‘misses’ a clock from the master due to noise or other bus errors, the device must continue to accept ‘in spec’ clocks and re-synch with the master on the next START or STOP condition.

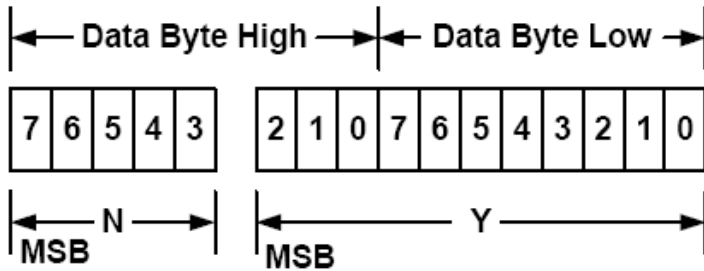
### 13.2.E Command

The following PMBus commands shall be supported for the purpose of monitoring currents, voltages, and power. All data should use the linear data format as documented in PMBus spec.

The Linear Data Format is a two byte value with:

- An 11 bit, two's complement mantissa and
- A 5 bit, two's complement exponent (scaling factor).

The format of the two data bytes is illustrated in Figure 4.



**Figure 4. Linear Data Format Data Bytes**

The relation between  $Y$ ,  $N$  and the “real world” value is:

$$X = Y \cdot 2^N$$

Where, as described above:

$X$  is the “real world” value;

$Y$  is an 11 bit, two's complement integer; and

$N$  is a 5 bit, two's complement integer.

Devices that use the Linear format must accept and be able to process any value of  $N$ .

<u>PMBus command</u>	Command Offset location	Byte size	<u>Description</u>
<u>CLEAR_FAULTS</u>	0x03	1	Writing any value into this byte will reset all the fault status
<u>PAGE_PLUS_WRITE</u>	0x05	variable	used with STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT
<u>PAGE_PLUS_READ</u>	0x06	Variable	used with STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT, STATUS_WORD
CAPABILITY	0x19	1	Provides a way for a host system to determine some key capabilities of a PMBus device
QUERY	0x1A	1 with block write read	Used to determine if the power supply supports a specific command
SMBALERT_MASK	0x1B	Variable	Used to prevent a warning or fault condition from asserting the SMBALERT# Signal. The masks can be changed by user.

VOUT_MODE	0x20	1	determines the format of Voltage output (Linear, direct, or VID), also set the mantissa
COEFFICIENT	0x30	5 with block write read	The system shall use this to read the values of m, b, and R used to determine READ_EIN accumulated power values.
FAN_CONFIG_1_2	0x3A	1	Returns the configuration of Fan 1 and Fan 2 in the power supply
FAN_COMMAND_1	0x3B	2	Allows system to request fans in the power supply to be set to the defined duty cycle. The system cannot cause the power supply fan to run slower than the power supply needs for cooling. This data should be in linear format. Example (32h=50% duty, 64h=100% Duty)
FAN_COMMAND_2	0x3C	2	Allows system to request fans in the power supply to be set to the defined duty cycle. The system cannot cause the power supply fan to run slower than the power supply needs for cooling. This data should be in linear format. Example (32h=50% duty, 64h=100% Duty)
STATUS_BYTE	0x78	1	command to report the On/off status of the power supply. Please refer to page 72 of PMbus spec part 2
STATUS_WORD	0x79	2	command to report the 2byte status of the power supply. Please refer to page 74 of PMbus spec part 2
STATUS_IOUT	0x7B	1	command to report the output current status
STATUS_INPUT	0x7C	1	command to report the input voltage and current status
STATUS_TEMPERATURE	0x7D	1	command to report the device temperature status
STATUS_FANS_1_2	0x81	1	command to report the fan status
READ_EIN	0x86	6	Command to report the accumulated input power (Total power usage since AC on)
READ_VIN	0x88	2	RMS input voltage in volts(note; not used on power distribution boards) Should reset to 0 when AC is lost
READ_IIN	0x89	2	RMS input current in amps (note; not used on power distribution boards) Should report 0 when AC is lost or in standby
READ VOUT	0x8B	2	12V Output Voltage (should reset to 0 during standby or AC is removed)
READ IOUT	0x8C	2	12V Output Current (should reset to 0 during standby or AC is removed)
READ_TEMPERATURE1 (Ambient)	0x8D	2	Read airflow inlet temperature (should be similar to the ambient temperature)
READ_TEMPERATURE2 (hot Spot)	0x8E	2	Read hotspot temperature (should be the hottest location inside the unit)
READ_FAN_SPEED_1	0x90	2	Returns the fan speed in RPM of fan sensor 1. This data should be in linear format
READ_FAN_SPEED_2	0x91	2	Returns the fan speed in RPM of fan sensor 2. This data should be in linear format
READ POUT	0X96	2	DC Output in Watts

READ PIN	0x97	2	AC input power in watts (note; not used on power distribution boards). Value should reset to 0W when in standby mode or AC is lost
PMBUS_REVISION	0x98	2	Reads the revision of the PMBus to which the device is compliant
APP_PROFILE_SUPPORT	0x9F	1	Defines that the power supply supports this application profile (default value 04h)
MFR_VIN_MIN	0xA0	2	Retrieves the minimum rated value, in volts, of input voltage (ex. 90Vac). This value remains a constant value.
MFR_VIN_MAX	0xA1	2	Retrieves the maximum rated value, in volts, of input voltage (ex. 262Vac). This value is a constant value.
MFR_PIN_MAX	0xA3	2	Retrieves the maximum rated value, in watts, of input power. If there is a high line or low line input power difference, the suitable input max power should be displayed properly. (ex. Power supply with rating 1000W@100-140Vac, 1200W@180-240Vac. During 100-140Vac, MFR_PIN_MAX=(1000W+10W fan DC power)/0.88 efficiency= 1148W. During 180-240Vac, MFR_PIN_MAX=(1200W+10W fan DC power)/0.9 efficiency=1345W)
MFR_IOUT_MAX	0xA6	2	Retrieves the maximum rated 12V output current
MFR_POUT_MAX	0xA7	2	Retrieves the maximum rated value, in watts, of output power. If there is a high line or low line input power difference, the suitable input max power should be displayed properly. (ex. Power supply with rating 1000W@100-140Vac, 1200W@180-240Vac. MFR_POUT_MAX should display 1000W or 1200W according to Vac input.
MFR_TAMBIENT_MAX	0xA8	2	Retrieves the maximum rated ambient temperature, in degree C, in which the unit might be operated. This value is a constant value. (default 50 Degree C)
MFR_TAMBIENT_MIN	0xA9	2	Retrieves the minimum rated ambient temperature, in degree C, in which the unit might be operated. This value is a constant value. (Default 0 Degree C)
MFR_MAX_TEMP_1 (Ambient)	0xC0	2	Retrieves the maximum rated ambient temperature (TEMPERATURE 1), in degree C, in which the unit might be operated. This value is a constant value. (default 50 Degree C)
MFR_MAX_TEMP_2 (hot spot)	0xC1	2	Retrieves the maximum rated temperature for the hotspot (TEMPERATURE 2), in degree C, in which the unit might be operated. This value is a constant value.

**CLEAR\_FAULTS Command definition:**

This will clear and reset all the fault and warning status bits to '0'.

**CAPABILITY command definition:**

**Table 7. CAPABILITY COMMAND Data Byte Format**

Bits	Description	Value	Meaning
7	Packet Error Checking	0	Packet Error Checking not supported
		1	Packet Error Checking is supported
6:5	Maximum Bus Speed	00	Maximum supported bus speed is 100 kHz
		01	Maximum supported bus speed is 400 kHz
		10	Reserved
		11	Reserved
4	SMBALERT#	0	The device does not have a SMBALERT# pin and does not support the SMBus Alert Response protocol
		1	The device does have a SMBALERT# pin and does support the SMBus Alert Response protocol

CAPABILITY default value:

Bits	Description	Value	Meaning
7	Packet Error Checking	1	Packet Error Checking is supported
6:5	Maximum Bus Speed	00	Maximum supported bus speed is 100 kHz
4	SMBALERT#	1	0= The device does not have a SMBALERT# pin and does not support the SMBus Alert Response protocol 1= It has SMBALERT#
3:0	Reserved	0000	reserved

**QUERY Command Definition:**

The QUERY command is used to ask a PMBus device if it supports a given command, and if so, what data formats it supports for that command. This command uses the Block Write-Block Read Process Call described in the SMBus specification, Version 2.0.

For the write portion of the process call, the one data byte is an unsigned binary integer, the value of which is equal to the command code requested to be investigated.

For the read portion of the process call, the one data byte is an unsigned binary integer with values as the following table.

### QUERY Command Returned Data Byte Format

Bits	Value	Meaning
7	1	Command is supported
	0	Command is not supported
6	1	Command is supported for write
	0	Command is not supported for write
5	1	Command is supported for read
	0	Command is not supported for read
4:2	000	Linear Data Format used
	011	Direct Mode Format used
	101	VID Mode Format used
	110	Manufacturer specific format used
1:0	XXX	Reserved for future use

If bit [7] is zero, then the rest of the bits are “don’t care”.

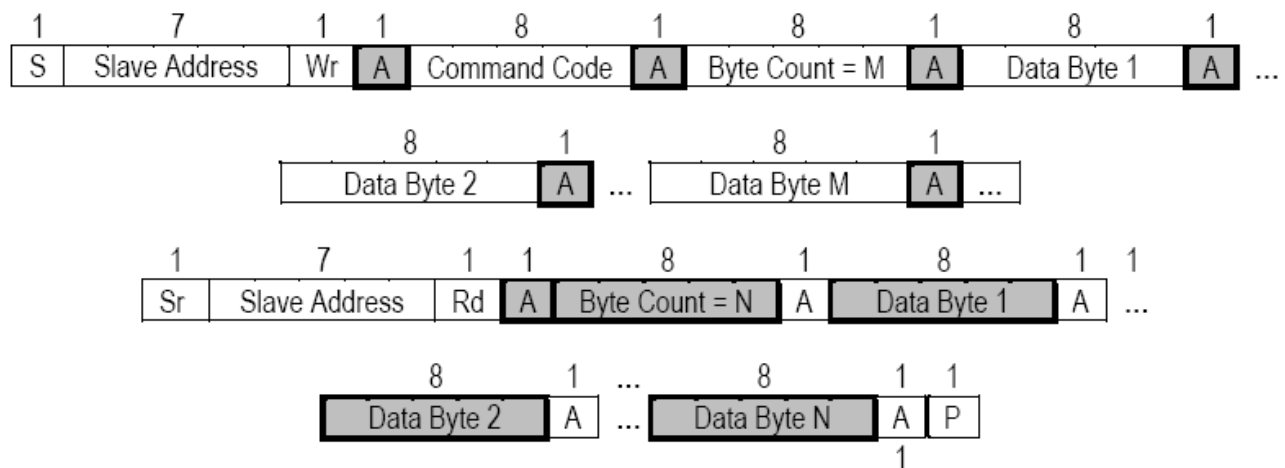


Figure 5-21: Block Write - Block Read Process Call

### SMBALERT\_MASK Command Definition:

The command format used to block a status bits from causing the SMBALERT# signal to be asserted. The bits in the mask byte align with the bits in the corresponding status register. For example, if the STATUS\_TEMPERATURE command code were sent with mask byte 01000000b, then an Over temperature Warning condition would be blocked from asserting SMBALERT#.

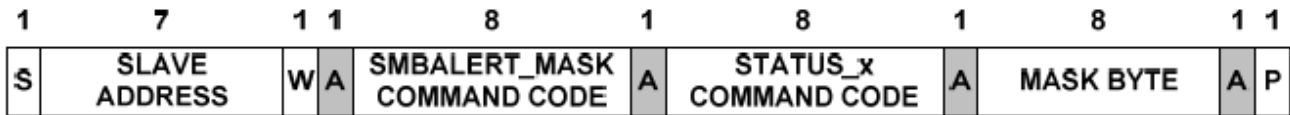


Figure 24. SMBALERT\_MASK Command Packet Format

The command format used by the host to determine the setting of the SMBALERT\_MASK for a given status register is shown in Figure 25.

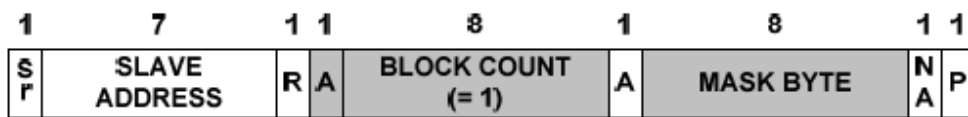
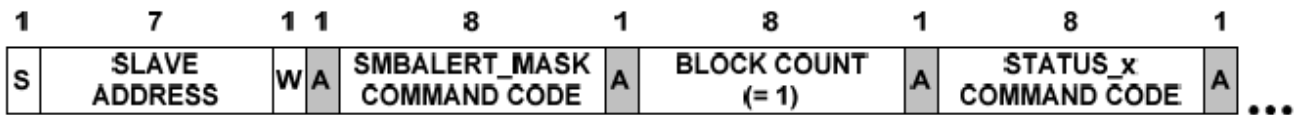


Figure 25. Retrieving The SMBALERT\_MASK Setting For A Given Status Register

**VOUT\_MODE Command Definition:**

For reading output voltages the power supply shall support the VOUT\_MODE command to report the output voltage formatting for the READ\_VOUT command. The VOUT\_MODE shall be set to Linear and the exponent (N) shall be set to -9.

VOUT\_MODE settings for reading output voltage(s).

Mode	Bits [7:5]	Bits [4:0] (N)
Linear	000b	10111b (-9)

**COEFFICIENT Command Definition:**

The system shall use this to read the values of m, b, and R used to determine READ\_EIN accumulated power values.

This command uses the Block Write-Block Read Process Call described in the SMBus specification, Version 2.0.

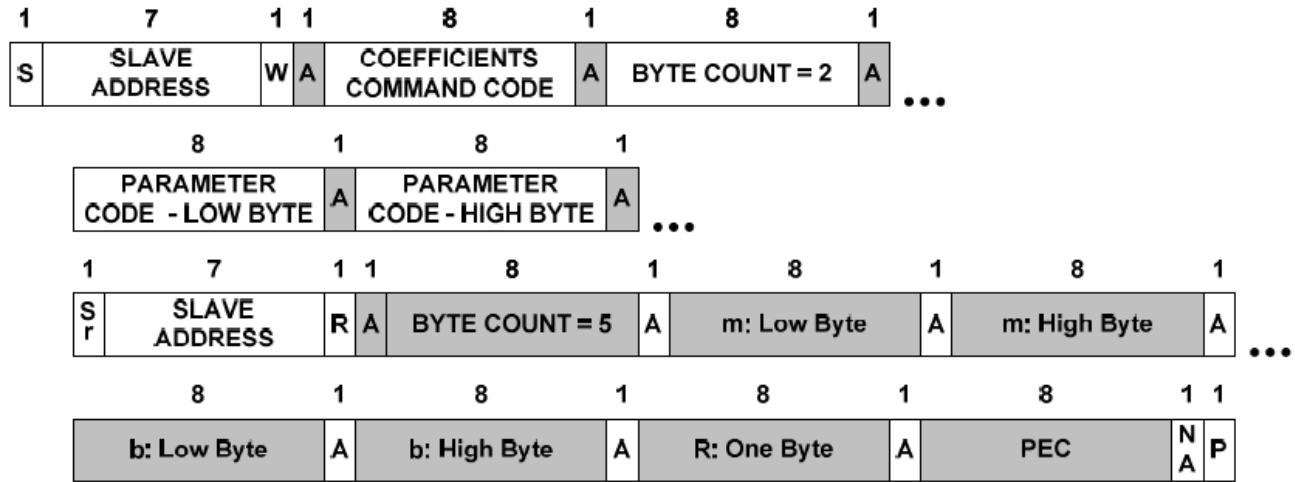
For the write portion of the process call, the byte count is two and there are two data bytes. The first data byte is the command of interest (ex. 0x95 for READ\_EIN). The second data byte indicates whether the host requesting the coefficients needed to encode a value to be written to the device or the coefficients needed to decode a value read from the device. A value of 01h in the second data byte indicates that the coefficients needed to decode a value read from the device are being requested. A value of 00h in the second byte indicates that the coefficients needed to encode a value for writing are being requested.

For the read portion of the process call, the byte count is five and the five bytes returned are (in this order):

- 1) Lower byte of m,
- 2) Upper byte of m,
- 3) Lower byte of b
- 4) Upper byte of b,

5) Single byte of R.

More information on the function and application of this command are given in Section 7.2. An example of the packet construction for retrieving the coefficients from a PMBus device using PEC is shown below.



**Retrieving Coefficients Using PEC**

The default values of m, b, and R shall be set to:

m=01h

b=00h

R=00h

**FAN\_CONFIG\_1\_2 & FAN\_CONFIG\_3\_4 Command Definition:**

Bit(s)	Default Value	Meaning
7	1	Fan 1 presence, 0=no fan1, 1=fan1 installed
6	0	Fan 1 commanded in RPM=1, commanded in duty cycle=0; Default is 0x0=duty command
5:4	0	Not used
3	1 or 0	Fan 2 presence, 0=no fan2, 1=fan2 installed
2	0	Fan 2 commanded in RPM=1, commanded in duty cycle=0; Default is 0=duty command
1:0	0	Not used

**FAN\_COMMAND\_1\_2 Command Definition:**

The system may increase the power supplies fan speed through using the FAN\_COMMAND Command. This command can only increase the power supply fan speed; it cannot decrease the power supply fan speed below what the power supply commands.

The control is configured to be duty cycle controlled using the linear format of the PMBus protocol.

The exponent N is fixed to a value of 0 (N=0). The command ranges from value 0000h (0% duty) to 0064h (100% duty).

**STATUS Commands:**

The following PMBus STATUS commands shall be supported. All STATUS commands except the STATUS\_FAN\_1\_2 and STATUS\_BYTE commands shall be accessed with the PAGE\_PLUS command since they are used by both the BMC and ME. The (BMC) and (ME) refer to the two instances of the command accessed via the PAGE\_PLUS command. The

status bits shall assert whenever the event driving the status bit is present. Once a bit is asserted it shall stay asserted until cleared using one of the five methods described below:

- 1) Writing a '1' to any given bit location shall reset on that bit of the command
- 2) Sending a CLEAR\_FAULTS command to the power supply shall reset all STATUS\_ bits to '0'
- 3) Cycling AC power OFF than ON shall reset all STATUS\_ bits to '0'
- 4) Systems with redundant power supplies where only one of the supplies cycle AC power OFF/ON; the power cycled power supply shall reset the STATUS\_ bits to '0' only when powered back ON. If the power supply is kept OFF, the STATUS\_ bits shall not be reset.
- 5) Cycling the PSON# signal from de-asserted to asserted shall reset the STATUS\_ bits to '0'. The bits shall be reset only on the assertion of PSON#, not the de-assertion.

**STATUS\_BYTE: Please refer to PMbus part 2 spec page 72.**

Offset 0x78		PAGEs 00h=BMC 01h=ME	SMBAAlert_MASK Default (0=causes assertion of SMBAAlert#, 1=does not cause assertion of SMBAAlert#)	
Bit #	7	Not used, default=0	00h, 01h	1
	6	Device is off due to PSON or for any reason (ex. Protection)=1, else 0	00h, 01h	1
	5	Output OVP=1, else 0	00h, 01h	1
	4	Output OCP=1, else 0	00h, 01h	1
	3	Vin under voltage=1, else 0	00h, 01h	1
	2	OTP=1; else 0	00h, 01h	1
	1	Not used, default=0	00h, 01h	1
	0	none of the above (Power is good and turned on)=1, else=0	00h, 01h	1

**STATUS\_WORD: Please refer to PMbus part 2 spec page 74.**

Byte	STATUS_WORD, Offset 0x79		PAGEs 00h=BMC 01h=ME	SMBAAlert_MASK Default (0=causes assertion of SMBAAlert#, 1=does not cause assertion of SMBAAlert#)
Low	7	Not used, default=0	00h, 01h	1
	6	Device is off due to PSON or for any reason (ex. Protection)=1, else 0	00h, 01h	1
	5	Output OVP=1, else 0	00h, 01h	1
	4	Output OCP=1, else 0	00h, 01h	1
	3	Vin under voltage=1, else 0	00h, 01h	1
	2	OTP=1; else 0	00h, 01h	1
	1	CML communication error=1, else 0	00h, 01h	1
	0	none of the above (Power is good and turned on)=1, else=0	00h, 01h	1
High	7	VOUT Fault=1, else 0	00h, 01h	1
	6	IOUT/POUT fault or warning=1, else 0	00h, 01h	1
	5	An input voltage, input current, or input power fault or warning=1, else 0	00h, 01h	1
	4	Not used, default=0	00h, 01h	1
	3	Power Good fault=1, else 0	00h, 01h	1
	2	Fan fault or warning=1, else 0	00h, 01h	1
	1	Not used, default=0	00h, 01h	1
	0	Not used, default=0	00h, 01h	1

**STATUS\_IOUT Command Definition:**

Bit	STATUS_IOUT, Offset 0x7B	PAGEs 00h=BMC 01h=ME	SMBAlert_MASK Default (0=causes assertion of SMBAlert#, 1=does not cause assertion of SMBAlert#)
7	IOUT Overcurrent Fault	00h, 01h	1
6	Not used, default=0	00h, 01h	1
5	IOUT Overcurrent Warning (>90% of rated output current)	00h, 01h	1
4	Not used, default=0	00h, 01h	1
3	Not used, default=0	00h, 01h	1
2	Not used, default=0	00h, 01h	1
1	POUT Overpower Fault	00h, 01h	1
0	POUT Overpower Warning (>90% of output power)	00h, 01h	1

**STATUS\_INPUT Command Definition:**

Bit	STATUS_INPUT, Offset 0x7C	PAGEs 00h=BMC 01h=ME	SMBAlert_MASK Default (0=causes assertion of SMBAlert#, 1=does not cause assertion of SMBAlert#)
7	VIN Over voltage Fault	00h, 01h	1
6	VIN Over voltage Warning (Vin>240Vac)	00h, 01h	1
5	Vin Under voltage Warning (Vin<90Vac)	00h, 01h	Page 00h=1; Page 01h=0
4	Vin Under voltage Fault	00h, 01h	1

3	Unit is off for insufficient Input Voltage (Input UVP)	00h, 01h	1
2	IIN Over current Fault	00h, 01h	1
1	IIN Over current Warning (when IIN over rated input current)	00h, 01h	1
0	Not used, default=0;	00h, 01h	1

**STATUS\_TEMPERATURE Command Definition:**

Bit	STATUS_TEMPERATURE, Offset 0x7D	PAGEs 00h=BMC 01h=ME	SMBAlert_MASK Default (0=causes assertion of SMBAlert#, 1=does not cause assertion of SMBAlert#)
7	Overtemperature Fault	00h, 01h	1
6	Overtemperature Warning	00h, 01h	Page 00h=1; Page 01h=0
5	Undertemperature Fault	00h, 01h	1
4	Undertemperature Warning	00h, 01h	1
3	Not used, default=0;	00h, 01h	1
2	Not used, default=0;	00h, 01h	1
1	Not used, default=0;	00h, 01h	1
0	Not used, default=0;	00h, 01h	1

**STATUS\_FANS\_1\_2 Command Definition:**

Bit	STATUS_FANS_1_2, Offset 0x81	PAGEs 00h=BMC 01h=ME	SMBAlert_MASK Default (0=causes assertion of SMBAlert#, 1=deso not cause assertion of SMBAlert#)
7	Fan 1 Fault=1, else=0	N/A	1
6	Fan 2 Fault=1, else=0	N/A	1
5	Not used, default=0;	N/A	1

4	Not used, default=0;	N/A	1
3	Fan 1 Speed Overridden (When User command is applied)=1; else 0	N/A	1
2	Fan 2 Speed Overridden (When User command is applied)=1; else 0	N/A	1
1	Not used, default=0;	N/A	1
0	Not used, default=0;	N/A	1

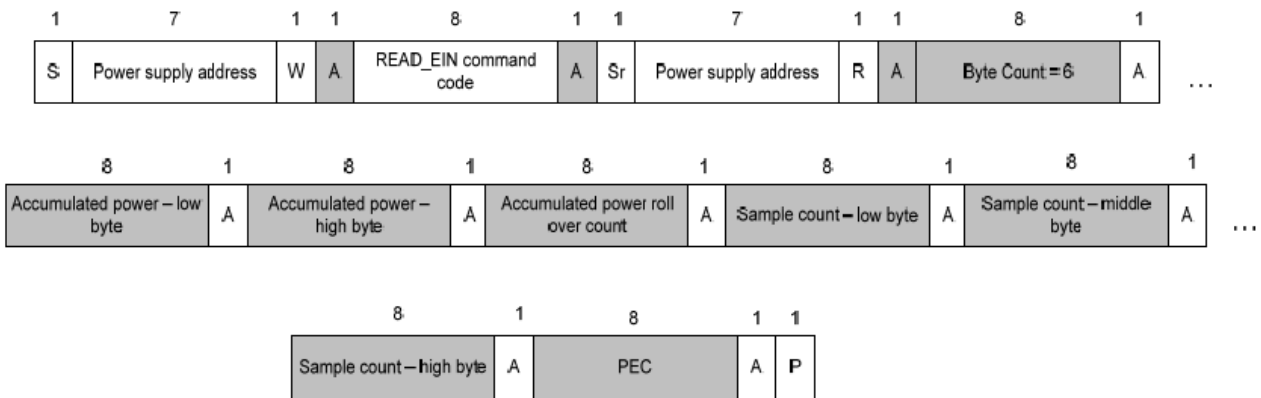
**READ\_EIN Command Definition:**

The READ\_EIN command shall use the PMBus direct format to report the accumulated power value and the sample count. The PMBus coefficients m, R, and B shall be fixed values and the power supply shall report these values using the PMBus COEFFICIENT command. The coefficient m shall be set to 01h, coefficient R shall be set to 00h, and coefficient b shall be set to 00h.

**READ\_EIN Requirements Summary**

	MIN	MAX	Description
Format	PMBus Direct format m = 01h, R = 00h, b = 00h		PMBus data format; refer to PMBus specification for details.
P <sub>sample</sub> averaging period	= 4 AC cycles		Period instantaneous AC power is averaged over to calculate P <sub>sample</sub> .
[P <sub>accum</sub> / N] Accuracy (10% to 19% load)	+/-15%		The calculated input power data shall meet these accuracy requirements over 100-240VAC and under the defined system polling rate.
[P <sub>accum</sub> / N] Accuracy (20% to 100% load)	+/-5%		
System polling rate	1 sample / sec	10 samples / sec	The power supply shall be polled over this range of rates while testing accuracy.

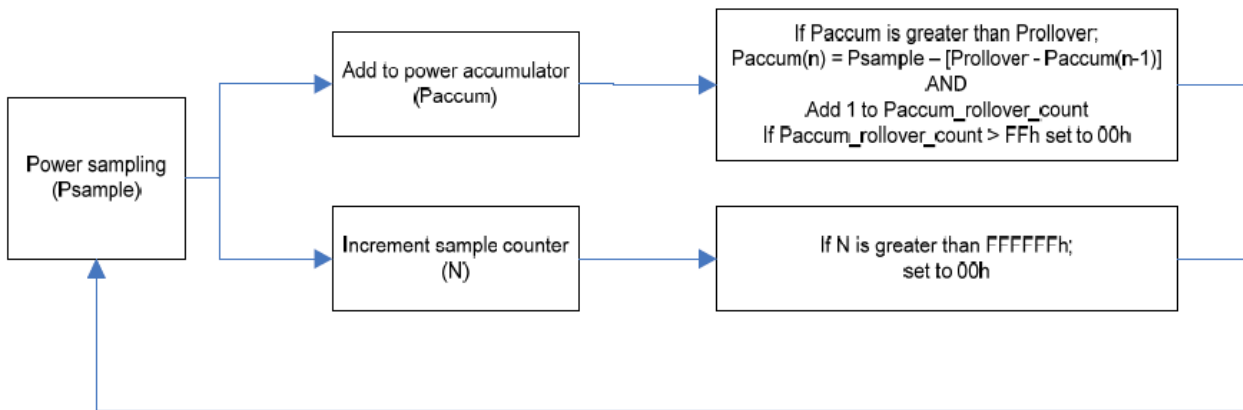
**READ\_EIN shall use the SMBus block Read with PEC protocol in the below format:**



**READ\_EIN Command**

**READ\_EIN Accumulators:**

The accumulated power data shall be the sum of input power values averaged over 4 AC cycles. The value shall automatically roll-over when the 15bit maximum value is reached (>7FFFh). The sample count should increment 1 for each accumulated power value. The system shall calculate average power by dividing the accumulated power value by the sample count. The system must sample READ\_EIN faster than the roll-over period to get an accurate power calculation. If the system sees a smaller value than the previous sampled data; then the system must account for the roll-over by adding 7FFFh to the present value. Below is a block diagram depicting the READ\_EIN accumulator function in the power supply.



Psample: ..... The sampled power value in linear or direct format

Paccum: ..... 2 bytes in PMBus linear or direct format.

The accumulated power values made up of Psample(0) + Psample(1) + ... + Psample(n)

N: ..... 3 byte unsigned integer value. The number of accumulated power values summed in Paccum

Prollover: ..... The max value of Paccum before a rollover will occur

Paccum\_rollover\_count: 1 byte unsigned integer counting the number of times Paccum rolls over.

Once this reaches FFh; it will automatically get reset to 00h

**READ\_EIN Power Supply Functional Diagram**

### Resetting READ\_EIN

The READ\_EIN power accumulator, roll-over counter, and sample count should keep the latest value when the power supply is put into standby mode. The power accumulator, roll-over counter and sample count should reset to 00 when AC power is lost.

### PMBUS\_REVISION Value:

Bits 7:5	Part I Revision	Bits 4:0	Part II Revision
0010	1.2	0010	1.2

### 13.2.F Manufacturer Specific Commands:

Offset 0xD0-0xDE is used to represent the unit model serial number. Data represented in byte format. These bytes are read/write capable through I2C

Below serial number is for example only:  
PWS-1K43F-1R

Offset	Serial number	
	character	Hex
D0	P	50
D1	1	31
D2	K	4B
D3	4	34
D4	6	36
D5	0	30
D6	9	39
D7	0	30
D8	1	31
D9	A	41
DA	0	30
DB	0	30
DC	0	30
DD	0	30
DE	1	31

Offset 0xE0 – 0xEB is used to represent the model number, data represented in byte format. These bytes are read/write capable through I2C.

PWS-1K43F-1R

Offset	Item number	
	character	Hex
E0	P	50
E1	W	57
E2	S	53
E3	-	2D
E4	1	31
E5	K	4B
E6	4	34
E7	3	33

E8	F	46
E9	-	2D
EA	1	31
EB	R	52

Additional information bytes for FRU backward compatibility. These bytes are read/write capable.

Offset	Function	Description
ED	Temperature upper limit	Internal temperature upper limit in degree Celsius. Direct data format, data length is one byte.
EE	Fan 1 pulse count lower limit	Value to represent the lower limit RPM of the power supply fan #1  The system software will convert this value, to fan RPM, using: RPM limit=(1/0.262) *(Fan Pulse Count limit * 60 /2)
EF	Fan 2 pulse count lower limit	Same calculation as fan 1. If fan 2 is not available, default value is 0x00.

Offset 0xF0-0xF5 is used to represent the unit revision number. Revision begins with Rev 1.0. Data is represented in byte format. These bytes are read/write capable using I2C.

Offset	Revision	
	character	Hex
F0	R	52
F1	E	45
F2	V	56
F3	1	31
F4	.	2E
F5	0	30

### 13.2.G Sensor Sampling

The sensor registers inside the power supply for monitoring input/output power, current, and voltage shall meet the following minimum requirements. Register refresh rate is the frequency the sensor register gets updated with a new measurement value.

Register refresh rate  $\geq$  10Hz

### 13.2.H Sensor Averaging

The sensor registers for monitoring input/output power, current, and voltage shall contained averaged data, not instantaneous peak data. This may be achieved in two ways; an arithmetic average or a low pass filter. An

exponential moving average shall not be used. The power supply shall refresh the sensor data at a rate no slower than the averaging duration.

READ\_PIN, shall be an average value over a 2 second interval.

READ\_IIN and READ\_VIN shall be an RMS value over a 2 second interval.

### 13.2.I Accuracy

The sensor commands shall meet the following accuracy requirements.

	10% of max load	20% of max load	50% of max load	100% of max load
READ_IIN	READ_IIN accuracy must be able to meet READ_PIN requirement below	+/-5%	+/-3%	+/-3%
READ_PIN	+/-5% or +/- 10W	+/-5%	+/-5%	+/-5%
READ_IOUT	+/-20%	+/-5%	+/-3%	+/-3%
READ_POUT	+/-5% or +/- 10W	+/-5%	+/-5%	+/-5%
READ_VIN	+/- 2% over full range			
READ_VOUT	+/- 2% over full range			
READ_TEMPERATURE	Required: +/-2 °C			

### 13.2.J Linearity

For any increase in actual power or current the resulting PMBus reading shall stay the same or increase. For any decrease in actual power or current the resulting PMBus reading shall stay the same or decrease.

### 13.2.K Resolution

The resolution of the PMBus input power sensor shall be no more than 3W. With an increasing or decreasing load in 1W steps; the associated power change using READ\_PIN shall not exceed 3W.

## 13.3 SMBAlert

The SMBAlert# Signal may be asserted (pulled low, less than 0.4V) by the power supply for any of the supported STATUS events. The events that control SMBAlert# can be masked during the SMBALERT\_MASK command. Default masking is shown in section 4.4.2.E of the status command definitions.

By default the SMBAlert# signal is asserted for the following cases:

- 1) AC Input voltage drops below the fault threshold (<90Vac) for more than 2ms.
- 2) Thermal sensor on a hot spot inside the power supply has exceeded it warning temperature (OTP temperature minus 3 degree C) for over 1sec.
- 3) Power supply is turned off due to PSON
- 4) Power Supply Fan fail
- 5) Power supply failure

The power supply does not support Alert Response Address (ARA). After asserting the SMBAlert# signal, the power supply shall keep its address at its standard address; not change to 18h.

The SMBAlert# signal shall be asserted whenever any un-masked event has occurred. This is a level detected event. Whenever the event is present SMBAlert# shall be asserted. If the SMBAlert signal is cleared, it shall immediately re-asserted if the event is still present.

The SMBAlert# signal shall be cleared and re-armed by the following methods:

- 1) Clearing STATUS bits causing the asserted SMBAlert# signal.
- 2) Power cycling with PSON or with AC power

### **13.4 Faults and Error Checking**

The power supply shall support PEC(packet error checking) per the SMBus 2.0 specification.

**Note:** \* The recommend level should cover 90% production.

## **14. Shock and Vibration**

### **14.1 Vibration**

Power supply should withstand a non-operational: Sinusoidal vibration, 1.0 G acceleration. 3-200Hz, sweep at 1/2 octave/min from low to high frequency, and then from high to low. Thirty minute dwell at all resonant points, where resonance is defined as those exciting frequencies at which the device under test experiences excursions two times larger than non-resonant excursions. Plane of vibration to be along three mutually perpendicular

### **14.2 Mechanical Shock**

The power supply will withstand the following imposed conditions without electrical or mechanical failure:

Non-operating Square Wave Shock: 40G, square wave at 200in/sec;on all six sides.

Non-operating half sine shock: Half Sine pulse for 70in/sec for 2ms; on all sides except top.

Operating half sine shock: Half Sine pulse for 40in/sec for 2ms; on all sides except top.

## **15. Mechanical Requirements**

### **15.1 Outline Drawing**

See drawing pdf included below.



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### **15.2 acoustic noise and Fan Speed Control**

Acoustic noise limitation: The acoustic noise level of PS stand-alone operation including stand-by operation must be less than 15dBa without fan. The vendors need to provide the test data of acoustic noise without fan for during DVT, PR stages

When AC plug in, Fans will be on and have minimum speed to cooling power supply to keep normal operating temperature. The power supply will have internally controlled PWM fans. The PWM fans will be thermal

controlled by microcontroller. Note that speed transition should be non-linear to reduce perceived noise from fan.

Fan control speed rule is shown in the attached file below.



PWM Fan Control  
Design Guideline 0.1.

### Fan Speed Control

The power supply will have two internally controlled 28mm fan. The fan will be 4 wires PWM Fan controlled by internal temperature and will have a slope of TBD.

### 15.3 Output Connector

The power supply will be fitted with powerblade FCI connector part no 51720-0601603AB type or equivalent. The connector includes 3 power pins for AC input, 14 signal pins and 6 power pins for 12V and return. See power supply mechanical drawing for dimensions.

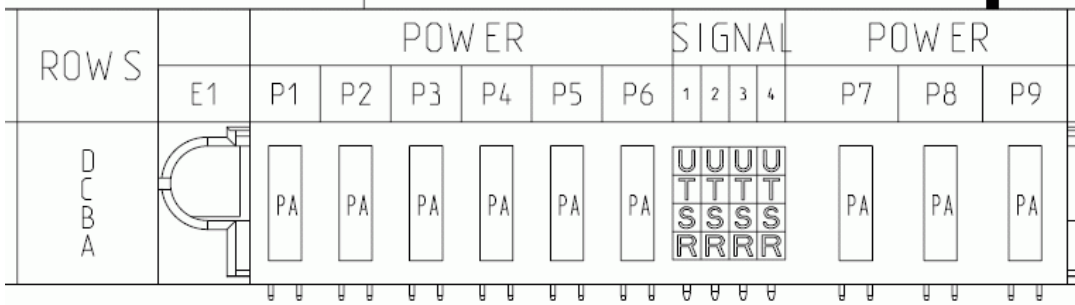


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### Power and Signal Connection

Pin #	Length	Description / NET	I/O
P1		+12Vo	analog O/P
P2		+12Vo	analog O/P
P3		+12Vo	analog O/P
P4		GND	analog O/P
P5		GND	analog O/P
P6		GND	analog O/P
D1	S	-RS (remote sense)	analog I/P
D2		+5Vsb	analog O/P
D3		+5Vsb	analog O/P
D4		+5Vsb (optional, must be open if not used)	analog O/P
C1		SCL	digital
C2		SDA	digital
C3		SIGNAL_GND (optional, must be open if not used)	digital
C4	S	PS_ON	TTL I/P
B1		DC_GOOD (early warning)	TTL O/P
B2	S	I_SHARE	analog O/P
B3	S	+RS (remote sense)	analog I/P
B4		SMBAlert	
A1		A0	digital
A2		A1	digital
A3		PRESENT	TTL O/P
A4		Reserved for power supply vendor	
P7		EARTH	Chassis GND
P8		NEUTRAL	power I/P
P9		LINE	power I/P

Length = S means the pin is 50 mil shorter than the longest pin



Barcode: P1K46CYWWRMSSSS

### 15.4 Product Labeling and Bar coding Requirements

Supermicro requires that the unit serial number be on both the power supply and matching outside carton/packaging.

### 15.5 Product Shipment Packaging

The power supply shipping package shall be design to provide protection from the environmental conditions it will be exposed from the manufacturing site to the final customer. The packaging shall be configured in a way that power supply can be individually packaged and shipped via normal parcel delivery or packaged in palletized format for high volume production shipment. The packaging shall comply with International Safe Transit Association (ISTA) procedures 3D and 3E.

### 15.6 Compatibility

No safety issue ( Cross Fire ) occurred when Swap in the redundant system with competitor PSU.

## 16 Redundancy Requirements

### 113.1 Current Sharing Operation

The power supply shall be designed for active current sharing.

Two or more than two power supplies will be paralleled in a system. Each power supply must be able to share load to within +/-10 % share error measured 25, 50, 100% of single power supply full load current. 5Vsb requires an "ORing" diode or FET to provide protection against internal short circuit fault.

### 113.2 Output Isolation Oring MOSFET

The 12V output current must pass through an Oring MOSFET to protect the bus voltage against a power supply internal fault.

### 113.3 Power Supply Behavior When Faulted

- 1 The faulted supply shall not sink more than 100 mA current.
- 2 I2C bus status shall be operational and valid, refer to "I2C Bus/VPD Interface".
- 3 The "DC Good" signal and "DC Good Fault" bit status shall be valid.

4 A power supply that fails due to a 12V or 5Vsb Over-Voltage condition will shutdown gracefully and will not cause shutdown of the other power supplies in parallel.

5 The power supply has to save 5 latest records of the abnormal shutdown on the EEPROM. The record is a byte data format, and its definition is shown below. The record should be clear before the shipping.

```
#define (reserved)                0x01
#define PRIMARY_OTP                0x02
#define SECONDARY_OTP             0x03
#define (reserved)                0x04
#define SCP_FAULT                 0x05
#define OCP_FAULT_220V            0x06
#define OCP_FAULT_110V           0x07
#define OVP_FAULT                 0x08
#define DC12V_OVP_FAULT           0x09
#define DC12V_UVP_FAULT           0x0A
#define AC_LOSS                   0x0B
#define FAN2_FAULT                0x0C
#define FAN1_FAULT                0x0D
#define OPP_FAULT                 0x0E
#define OTHER_FAULT               0x0F
```

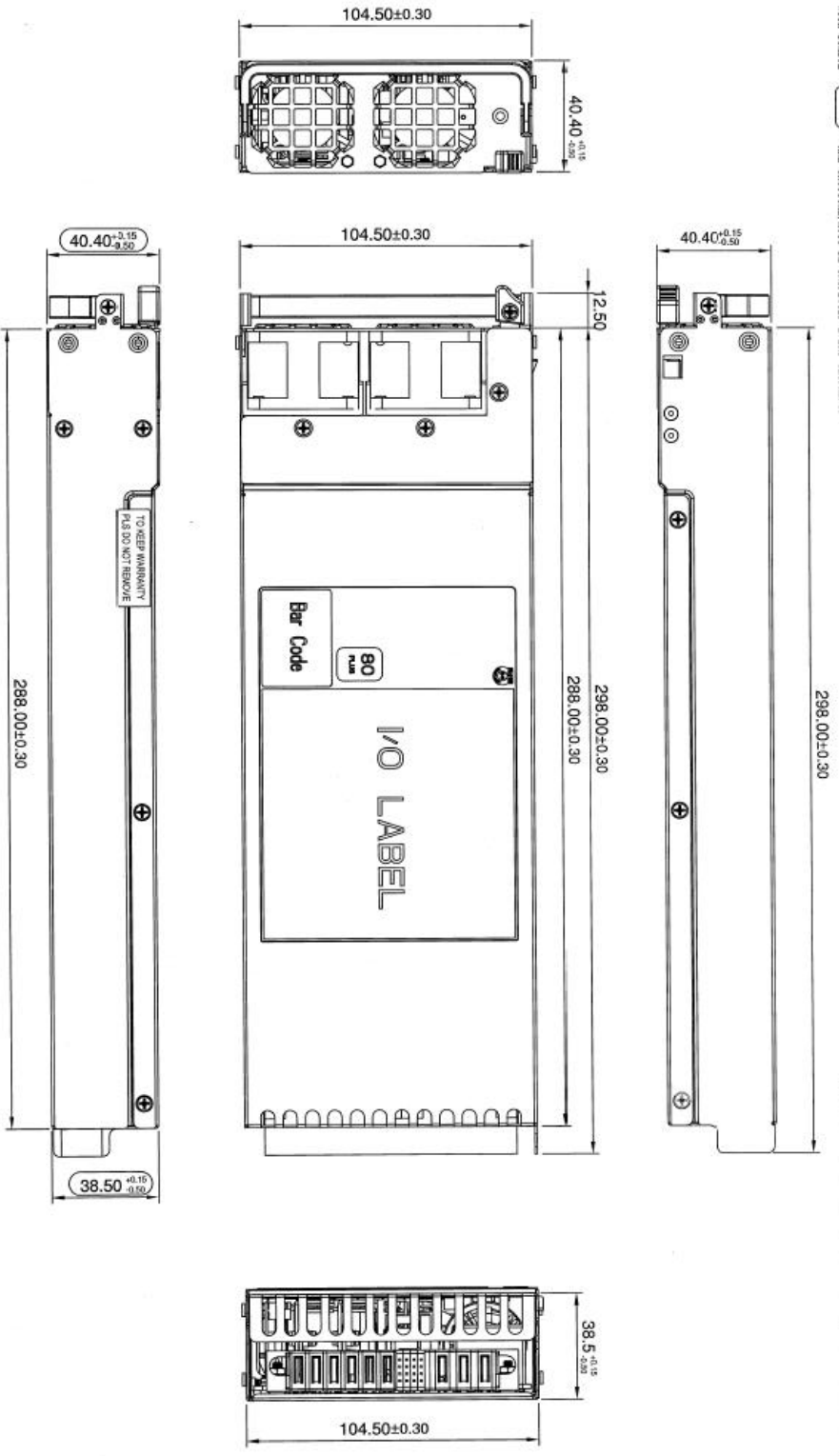
#### 4.4 Parallel Stability

The power supply shall be unconditionally stable under all system load and AC line conditions while operating alone or in parallel mode.

#### 113.5 Hot Swap

The power supply must be designed with “hot swap” function with or without active AC line cord. After Hot swap I2C address shall be same as host power supply backplane hardware assigned. Host existing working power supply shall not be affected by hot swapping power supply.

- NOTES:
1. INTERPRET DIMENSIONS PER CNS.
  2. DIMENSIONS NOT SHOWN OR HAVING SHALL REFER TO A GENERAL TOLERANCE.
  3. ALL EXPOSED EDGES MUST HAVE THE REQUIREMENTS SPECIFIED IN CL 1489.
  4. MATERIAL SURFACE AND INTERIOR SURFACE OF HOLES TO BE FREE OF OIL, NICKS, BURRS AND RESIDUE.
  5. ALL COMPONENTS AND THEIR MANUFACTURING PROCESS SHALL BE FULL MARKS.
  6. DIMENSIONS WITH SYMBOL "C" ARE CRITICAL, MUST BE INSPECTED EVERY SHIPMENT.



REV.	Description	Modify By	Modify Date	Assemble Basis	QTY. No.
Δ	Release	C. K.	2011.08.22	-	-
Δ	-	-	-	-	-
Δ	-	-	-	-	-

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**COMPUWARE** COMPUGRAPH TECHNOLOGY CO., LTD.

Model: CPR-1421-5M1 (PMS-1K43F-1R)  
 Part No.: CPR-1421-5M1 (V1.0)

Title: OUTLINE DRAWING

Scale: 1:1.5

Material: -  
 Finish: -  
 Units: mm

Version: 1.0

Author: C.K. Ohnig  
 Date: 1/10/10

Approved: [Signature]  
 Date: 1/10/10

Reviewed: [Signature]  
 Date: 1/10/10

Checked: [Signature]  
 Date: 1/10/10

Drawn: [Signature]  
 Date: 1/10/10

Material: -  
 Finish: -  
 Units: mm

Scale: 1:1.5

Version: 1.0

Author: C.K. Ohnig  
 Date: 1/10/10

Approved: [Signature]  
 Date: 1/10/10

Reviewed: [Signature]  
 Date: 1/10/10

Checked: [Signature]  
 Date: 1/10/10

Drawn: [Signature]  
 Date: 1/10/10