COMPUWARE
肯 微 科 技 股 份 有 限 公 司

Document Name
Product Specification

Release Document

Compuware Project Name	CPR-1421-1M2LF	Revision	4
Customer Project Name		Date	2011-12-28
Component P/N		Page	28

History Record		
Date	Description	Revision
2009-06-03	Change Fan to 4 wires PWM Fan Add Compatibility Gold Level Efficiency Update output power and efficiency Update Timing request Revise AC input voltage on/off range Release for Pilot Run	1
2009-10-29	Update PMbus 1.1 version Add +12V on DC_Good Pin#B1 Add Outside dimension drawing Add +5Vsb rising time and +12V rising time spec. to meet SSI & ATX	2
2010-02-25	Update Outside dimension drawing(80 plus lable)	3
2011-12-28	Adjust DC_GOOD on timing to 50ms~120ms from +12V within regulation	4

Approved By	**Signing By**	**Prepared By**
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1. Introduction

This document contains technical specification for 1.4KW 1U AC-DC power supply. The power supply will be packaged in 1U height with 12.85 inch length and 3.95 in width. The power supply will accept a wide input voltage range of 90 to 264Vac, while providing precisely regulated 12Vdc output voltage of 1.2KW at 115Vac and 1.4KW at 230Vac. The power supply will encompass all protective features and conform to safety agency regulatory requirements. The power will be designed for redundant operation and includes an active Or'ing circuit for isolation. I2C circuit protocol will be included to interface with external devices for communication.

2. Target Cost

The target manufactured cost for AC – DC 1U power supply is $135. This includes material, labor and load.

3. Technical documentation deliverables

1. Design verification Test Report. –
2. Qualification Report
3. Manufacturing Qualification Report
4. Safety Agency Compliance
5. Component Stress Analysis – This should include measurements on power train critical components against CW design margins. Should include turn on and off measurements (waveforms where applicable) at full and light load and at temperature (-5, ambient and 50℃) where applicable . Please refer to the embedded document for further details

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6. Reliability Verification Report – Refer to section 13.7
7. Engineering Samples with technical datasheet
8. Manufacturing/quality Audit
9. Production Schedule

4. Electrical specification

Table 1 **Input voltage specification**

Characteristics	Conditions	Min	Typ	Max	Units
Input voltage range		90	120/240	264	V_{ac}
Input current	Full load @ 100VAC			15	A
Input Frequency		47	50/60	63	Hz
Input voltage power-on	Must have a minimum 2V of hysterisis between off	82		90	V_{ac}
Input voltage power-off	Must have minimum 2V of hysterisis between on	73		83	V_{ac}
Inrush current	First half cycle			25	A_{pk}
Input over current protection	In-line fuse			20	A
Power Factor Correction	All specified input AC voltage; Full load/ >25% Iout		≥0.95/ ≥0.75		

Table 2 Output Voltage specification

Characteristics	Conditions	Min	Typ	Max	Units
Output voltage set point	Nominal line@full load	11.95	12	12.05	V_{dc}
Output Power	@230Vac			1400	W
Output Power	@115Vac	1200			W
Output current		1		117	A
Line/Load Regulation		11.52		12.6	V
Standby Voltage					
5.0V set point	5V	4.95	5.0	5.05	V
Standby current		0		6	A
Standby line/load reg		4.8		5.25	V
Ripple & noise 12Vout 5VStandby	V_{in} = 90-264V_{ac}; Full load; 20MHz Bandwidth; Co = 0.1µF ceramic + 10µF tantalum			 120 50	 mV mV
Transient Response	12Vo→50% max step load@ 0.5A/µs, 2200µF capacitive load 5Vsb→25% max step load @0.5A/µs, 1µF cap load	11.52 4.8		12.6 5.25	V V

Table 3 Protection Characteristics

Characteristics	Conditions	Min	Typ	Max	Units
Output current limit 12V 5Vsb		 130 7		 160 9	 A A
Output short-circuit current	Resistance 0.1 ohm or less	Latch-off			
Over voltage protection 5V standby				14.5 6	V_{dc} V_{dc}
Output under voltage limit		10.5			V_{dc}
Over temperature protection	Based on temperature limiting component		TBD		°C

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Table 4 Feature Characteristics

Characteristics	Conditions	Min	Typ	Max	Units
AC on Delay	V_{in} → output regulation range			2500	ms
Hold up time	V_{in} =90 – 264Vac; 75% load	20			ms
Active Load share Accuracy	Compensation for positive rail only; For +25% to 100% full load current			±10	$\%I_{o,\ rated}$
Capacitive load 12V 5Vsb		 1K 100		 40K 1K	 µF µF
On/off# Output enable (on) Output disable (off)	 Signal pulled low Signal pulled high (open)	 2.0		 0.8	 V V
DC good signal	Open collector DC Good → signal pulled high				
LED DC good LED AC/5Vsb good LED	 Green color Amber color				

5. AC Requirements

5.1 AC Input

The power supply shall operate over wide input voltage range and line frequency described in input specification table.

5.2 AC Input Connector

The AC input connection shall be accomplished in combination with DC output connector (FCI P/N 51720-0601603AB). The AC section of the inlet is rated for 15A/250Vac or greater than 14A. Refer to the power supply mechanical drawing for the physical location of the AC input/DC output connector.

5.3 Harmonic Current

This power supply shall meet latest EN61000-3-2/-3 requirement for ITE instrument. When measured at full output load and 50% of full output load.

5.4 Input under/over voltage protection

The power supply shall shutdown when the input voltage is under or over the shutdown threshold limits (268 to 275Vac). The power supply shall recover automatically when the input voltage is restored to normal operation limits. There shall be sufficient hysteresis build in circuit to ensure no oscillation is observed. The power supply shall issue noted alarms to provide status until input AC voltage is completely removed.

5.5 AC Inrush Current

After AC power is applied to the power supply, any initial inrush current surge or spike of first half cycle shall not exceed 25 amps peak. All internal components (including the fuse, bulk rectifiers and surge limiting device) must be able to withstand the surge current without damage, the peak inrush current shall be less than the ratings of its critical components for all conditions of line voltage, as defined in "AC Input", and during the power line disturbances specified in section "**Power Line Disturbance Requirements**". Repetitive On/Off cycling of the AC mains shall not damage the power supply. The inrush current limit impedance shall be bypassed by either a relay contact or other low impedance device during normal operation.

5.6 Power Factor Correction

The power supply must exhibit a power factor equal to or better than 0.997 at any input mains voltage and measured at full rated load. For any load less than maximum, the apparent power shall never exceed the maximum load apparent power. Furthermore, for any load greater than 20% of maximum (as described in DC Load Requirement), the power factor total harmonic current distortion THD must be less than 10%

5.7 AC line isolation

The primary and secondary circuit shall be electrically isolated from each other and from the case. The power supply shall meet all safety agency requirements for dielectric strength including reinforced insulation per standard UL60950 and IEC60950.

6. Output Requirements

6.1 DC output voltage

The power shall be designed to provide precisely regulated single output as defined in specification table.

6.2 DC output power

The power supply shall be capable of delivering full 1.2KWatts at the 115Vac input voltage and 1.4KWatts at the 230Vac input voltage.

6.3 DC output regulation

The power supply shall comply with regulation limits listed in specification table. Regulation shall be measured at the termination points of the remote sense leads. This limit shall be maintained under following list of conditions.

- Input AC line voltage changes due to steady state variation from minimum to maximum as specified in **AC Input**.
- Input line voltage transients.
- Load changes as defined in specification table.
- Interactions between outputs as a function of their loads (including dynamic and static loads).
- Ripple voltage as defined in section "**output ripple & noise**".
- Component changes due to manufacturing tolerances
- Component changes due to aging.
- Component changes due to self-heating (warm-up drift)
- Environmental changes within the bounds specified for ambient temperature, altitude, airflow and vibration.
- The step load may be applied to any static combination defined in Sections "**output transient response**".

6.4 Output Remote sense

The 12V output shall have provision for remote voltage sense. With the remote sense connected to the assigned voltage wire, the regulation limits specified in the specification table applies. The remote sensing must be able to compensate for a maximum voltage drop of 300 mV on the positive voltage distribution rail. When the remote sense wires are disconnected from the remote sense point, a default sensing location will be the output connector the power supply.

6.5 Output ripple & noise

The power supply shall comply with the specified limits over the entire range of operating conditions. The output voltage ripple shall be measured at the pins of the mating output connector. Ripple is defined as an AC differential voltage between the output voltage pins and return pins, that is present on the power supply output. This definition includes, but is not restricted to, AC voltage that is due to line voltage ripple, switching frequency ripple and dynamic loading. For the purpose of this measurement, the remote sense wires will be tied the output voltages directly at the pins of the mating output connector. Ripple voltage shall be measured with a 0.1 uF ceramic capacitor in parallel with a 10 uF electrolytic capacitor connected between the measured voltage and its return. Conformance to this requirement shall be measured using a differential amplifier with 20 MHz bandwidth.

6.6 DC Common to Frame Connection

DC common shall be connected to frame ground in the power supply.

6.7 Output transient response

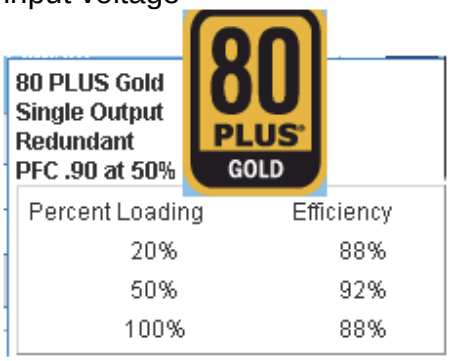
The power supply shall maintain compliance to the specified limits during a dynamic load condition. The output shall remain within the specified limits for the step loading and within the limits specified in below table. The load transient repetition rate shall be tested between 50 Hz and 5 KHz at duty cycles ranging from 10% - 90%. The step load may occur anywhere within the min load to the max load, but the peak load will not be over 25% of max load.

Transient load requirements

Output	Step load size	Load slew rate	Capacitive load
12V	50% of max load	0.5A/us	3000uF
5Vsb	25% of max load	0.5A/us	1uF

6.8 Efficiency

The power supply efficiency (watts output/watts input) shall be equal to or greater than 92% at the 50% of maximum load defined in Gold Level specification table with 230VAC input voltage



6.9 Stability

The power supply shall maintain stable operation over all conditions listed below. The phase margin must be a minimum of 45° where the gain is less then or equal to 1.

- DC and dynamic loads as defined in their respective sections.
- All input conditions as defined in section "**AC Input**"
- All environmental conditions as defined in section "**Environmental Requirements**"
- All load capacitance ranges as defined in section "**Load Capacitance**"
- The power supply must also be stable when powering a negative impedance load such as Voltage Regulation Module (VRM).
- The gain and phase plots using actual VRM and hard disk drive loads have to be taken and should meet 45 degree phase margin requirement.

6.10 Output voltage overshoot at start up and shutdown

During start up, the output voltage shall rise monotonically to within 5% of Vo, rated and must be in regulation band within 50 ms. During shutdown, the output voltage shall be within 5% of rated output and decay monotonically to ground level. There shall be no positive excursion during shutdown.

6.11 Output No Load Operation

If the load is removed from the output, the following must be maintained:

- No internal component stressed beyond its rating.
- The supply must start up and operate.

This condition shall cause no damage to the power supply. Protection circuits must not disable the power supply. The power supply shall operate with no load on all DC outputs. Output regulation may be relaxed to +/-20% during this condition, however **DC GOOD signal must stay high**. Protection circuits must not be disabled in this mode of operation.

6.12 Residual Voltage

The residual voltage at 12V output for no load condition shall not exceed 100mV when AC voltage is applied to the supply under DC "OFF" condition.

6.13 Output Repetitive Step Load

The output shall withstand a peak step load defined by the following conditions:
1) The summation of the average value of the step load and the static load shall not exceed 100A.
2) Step peak amplitude shall not exceed 125A.

6.14 Output Reverse EMF

The power supply shall be able to start even if there is a **Reverse EMF** of up to 3V on +12V output:
1) After initial startup.
2) After the power supply is turned off using either the "On/Off#"
3) After removing AC power and then reapplying.

6.15 Load Capacitance

For stability and power up considerations, the maximum and minimum load capacitance is as follows

Load Capacitance		
Voltage	Minimum capacitance	Maximum capacitance
+12V	1000 µF	40,000 µF
+5Vsb	100 µF	1,000 µF

7. Protection Requirement

7.1 Primary Protection

The supply must have internal primary over-current protection. A normal blow fuse must be placed in the line side of the input circuit. The input power line must be fused in accordance with the safety requirements of section "**Safety**". The input fuse must be rated at 20A or less. This fuse is not to be considered replaceable for purposes of determining power supply reliability and operating life as specified in section.
If any component on the line side of the fuse is shorted or opened, it may not cause a fire or any other safety risk. The fuse must be approved by UL, CSA and SEMKO. The PC board must be labeled "Replaced only with (YYYYYY) P/N XXXXXX".

YYYYYY= Fuse Vendor Name XXXXXX=Fuse Vendor Part Number

7.2 Secondary Protection

7.2.1 Shutdown Definition

Shutdown is defined as a condition where the 12V output latches off. 5Vsb shall remain on. The shutdown latch shall be reset by either removal of the AC input power or changing the "**On/Off#**" signal state. The power supply shall not latch off because of under voltage condition on the output unless it is caused by an overload condition.

7.2.2 Output over current protection

The power supply shall include current limit circuit to provide protection against over load condition. In an event of output current exceeds the over current limit threshold defined in specification table, the output will latch-off and remain off. The output shall be recovered per shutdown definition. During such event, the standby must remain ON unless the fault is cause by standby over load condition. For standby overload condition, current fold back method is preferred. The standby output should not latch off. The standby must return to normal operation once the fault is removed.

Notes:

1) Over current on the output must not trip due to dynamic characteristics of the +12V load, as defined in transient response section.

2) The power supply shall shut down when an applied 10A per second ramp reaches the maximum continuous current trip point.

7.2.3 Short circuit protection

The power supply shall latch off and suffer no physical damage when the output is shorted to its DC return, however 5Vsb should continue to operate normally under this condition. The power supply shall not latch off if 5Vsb signal shorts to its DC return. A short circuit is considered to be resistance of 0.1 Ohms or less.

7.2.4 Output over voltage protection

The power supply shall include an independent protection circuit that provides protection in an event of over voltage condition at the output connector.

In an event of over voltage condition, the power supply must shutdown and latch off. 5Vsb must continue to operate normally.

Over voltage protection circuits shall not cause the power supply to shutdown as long as the output voltages are within regulation limits.

The protection circuitry must be independent from the regulation circuitry including voltage references and secondary-primary feedback elements.

No single component failure may cause a sustained over voltage.

Note: A shutdown caused by an over voltage in one power supply will not cause the other power supply in parallel to shutdown.

7.2.5 Output under voltage protection

The power supply shall not latch off due to Under-Voltage condition on any one of the outputs unless it is caused by an overload condition on the output. Under voltage circuits shall not cause the supply to shutdown as long as the output voltages are within regulation limits. The protection circuitry must be independent from the regulation circuitry, including voltage references and secondary-primary feedback elements.

7.2.6 Over temperature protection

A temperature sensing device, or devices, internal to the power supply shall monitor critical component(s) temperature(s). If monitored component(s) critical temperature(s) is (are) reached, the power supply shall stay in regulation for 30 seconds then latch off all outputs except +5Vsb. The critical temperature is to be determined (TBD).

7a. I^2C and PMBus™ 1.1 standard.

I^2C interface has to meet Super Micro standard and PMBus™ 1.1 standard

7a.1 Salve address will be 0x70 (default), 0x72, 0x74, 0x76

All the data follows FRU spec.

There is an Internal Area in FRU that is used and defined by vendor (us). Therefore,
We use it for health monitoring. It is located in second block (offset 0x08),
Offset 0x09: Temperature,
Offset 0x0A: Fan 1 speed,
Offset 0x0B: Fan 2 speed,
Offset 0x0C: Power Status,
Offset 0x0D: Temperature High Limit,
Offset 0x0E: Fan 1 speed Low Limit,
Offset 0x0F: Fan 2 speed Low Limit.
Offset 0x16: Firmware Version (for example, revision 2.1 would be 0x21).
Offset 0x10-0x15 and 0x17: reserved for future use.

Power Status: bit0 =1 -> GOOD, bit0 = 0 -> Failed
Fan Speed formula: RPM = (1/0.262) *(Fan Pulse Count * 60 /2)

User want to retrieve the FRU data, must follow FRU spec.

Power supply I2C operation shall not latch system I2C bus for over certain time period needed for normal operation. Power supply I2C shall have auto reset function in case of waiting for clock pulse over a reasonable time period.

7a.2 PMBus

The PMbus firmware version of the power supply shall follow the

1. PMBus Power System Management Specification Part I – General Requirements, Transport and Electrical Interface.
2. PMBus Power System Management Specification Part II – Command Language

The device in the power supply shall be compatible with both SMBus 2.0 'high power' specification for I^2C V_{dd} based power and drive (for Vdd = 3.3V). This bus shall operate at 3.3V but be tolerant of 5V signaling.

One pin is the Serial Clock [SCL] (PSM Clock). The second pin is used for Serial Data [SDA] (PSM Data). Both pins are bi-directional, open drain signals, and are used to form a serial bus. The circuits inside the power supply shall derive their power from the standby output.

The device shall support SMBus clock-low timeout (Ttimeout). This capability requires the device to abort any transaction and drop off the bus if it detects the clock being held low for >40ms, and be able to respond to new transactions 10ms later.

The device must recognize SMBus START and STOP conditions on ANY clock interval. (These are requirements of the SMBus specifications, but are often missed in first-time hardware designs.) The device must not hang due to 'runt clocks', 'runt data', or other out-of-spec bus timing. This is defined as signals, logic-level glitches, setup, or hold times that are shorter than the minimums specified by the SMBus specification. The device is not required to operate normally, but must return to normal operation once 'in spec' clock and data timing is again received. Note if the device 'misses' a clock from the master due to noise or other bus errors, the device must continue to accept 'in spec' clocks and re-synch with the master on the next START or STOP condition.

7a.3 Addressing

System addressing Address2/Address1/Address0	0/0/0	0/0/1	0/1/0	0/1/1
Power supply PMBus™ device	78h	7Ah	7Ch	7Eh

Note: Non-redundant power supplies will use the 0/0/0 address location.

7a.4 Command

The following PMBus commands shall be supported for the purpose of monitoring currents, voltages, and power, the detail definition is defined by PMBus™ 1.1 standard.

PMBus command	Description
READ_IIN	RMS input current in amps (note; not used on power distribution boards)
READ_VIN	RMS input voltage in volts(note; not used on power distribution boards)
READ PIN	AC input power in watts (note; not used on power distribution boards)
READ_VOUT	DC 12V output voltage in volts, the format is set by the VOUT_MODE command.
READ_IOUT	DC 12V output current in amps.
READ_POUT	DC output power in watts.

VOUT_MODE Command to report the output voltage formatting for the READ_VOUT command.
STATUS_BYTE Command to report the On/off status of the power supply. Please refer to page 74 of PMbus spec part 2
READ_TEMPERATURE Read airflow inlet temperature

7a.5 Accuracy

READ_TEMPERATURE	Desired: +/- 1ºC Required: +/-3 ºC

All data response from PMbus command, except STATUS_BYTE and manufacturer specific commands, are represented in linear format as defined in PMBus spec part 2.

STATUS_BYTE: Please refer to PMbus part 2 spec page 72.

Offset 0x78		
Bit #	7	Not used, default=0
	6	Device is off due to PSON or for any reason (ex. Protection)=1, else 0
	5	Output OVP=1, else 0
	4	Output OCP=1, else 0
	3	Vin under voltage=1, else 0
	2	OTP=1; else 0
	1	Not used, default=0
	0	none of the above (Power is good and turned on)=1, else=0

7a.6 Manufacturer Specific Commands:
Offset 0xE0 – 0xEB is used to represent the model number, data represented in byte format. These bytes are read only through I2C/PMbus.

	Item number	
Offset	character	Hex
E0	P	50
E1	W	57
E2	S	53
E3	-	2D
E4	1	33
E5	K	4B
E6	2	32
E7	1	31
E8	P	50
E9	-	2D
EA	1	33
EB	R	52

Offset 0xF0-0xF5 is used to represent the unit revision number. Revision begins with Rev 1.0. Data is represented in byte format. These bytes are read/write capable using I2C.

	Revision	
Offset	character	Hex
F0	R	52
F1	E	45
F2	V	56
F3	1	31
F4	.	2E
F5	0	30

7a.7 Sensor Sampling

The sensor registers inside the power supply for monitoring input/output power, current, and voltage shall meet the following minimum requirements. Register refresh rate is the frequency the sensor register gets updated with a new measurement value. Sensor averaging duration is the time over which the data shall averaged to obtain the value of the registers value.

Register refresh rate ≥ 10Hz
Sensor averaging duration; ≤ 100msec, ≥ 10msec

7a.8 Accuracy

The sensor commands shall meet the following accuracy requirements.

	20% of max load	50% of max load	100% of max load
READ_IIN (at low line input)	+/-4%	+/-2%	+/-2%
READ_IIN (at high line input)	+/-4%	+/-2%	+/-2%
READ_PIN	+/-7%	+/-5%	+/-5%
READ_IOUT	+/-2%	+/-2%	+/-2%
READ_POUT	+/-3%	+/-3%	+/-3%

READ_VIN	+/- 2% over full range
READ_VOUT	+/- 2% over full range
READ_TEMPERATURE	Desired: +/- 1ºC Required: +/-3 ºC

8. Power Supply Sequencing

Power supply output voltages timing shall follow signal requirement section of this document and 6.11 of SSI ERP2U power supply design guide, V2.0, except for 5V, 3.3V, and –12V (See Below).

6.11 Timing Requirements

STATUS
Required

These are the timing requirements for the power assembly operation. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 200ms. The +3.3 V, +5 V and +12 V output voltages should start to rise at about the same time. All outputs must rise monotonically. The +5 V output needs to be greater than the +3.3 V output during any point of the voltage rise. The +5V output must never be greater than the +3.3V output by more than 2.25 V. Each output voltage shall reach regulation within 50 ms (T_{vout_on}) of each other during turn on of the power supply. Each output voltage shall fall out of regulation within 400 ms (T_{vout_off}) of each other during turn off. Figure 2 and Figure 3 show the turn ON and turn OFF timing requirements. In Figure 3, the timing is shown with both AC and PSON# controlling the ON/OFF of the power supply.

Table 24: Output Voltage Timing

Item	Description	MIN	MAX	Units
T_{vout_rise}	Output voltage rise time from each main output.	5	200	ms
T_{vout_on}	All main outputs must be within regulation of each other within this time.		50	ms
T_{vout_off}	All main outputs must leave regulation within this time.		400	ms

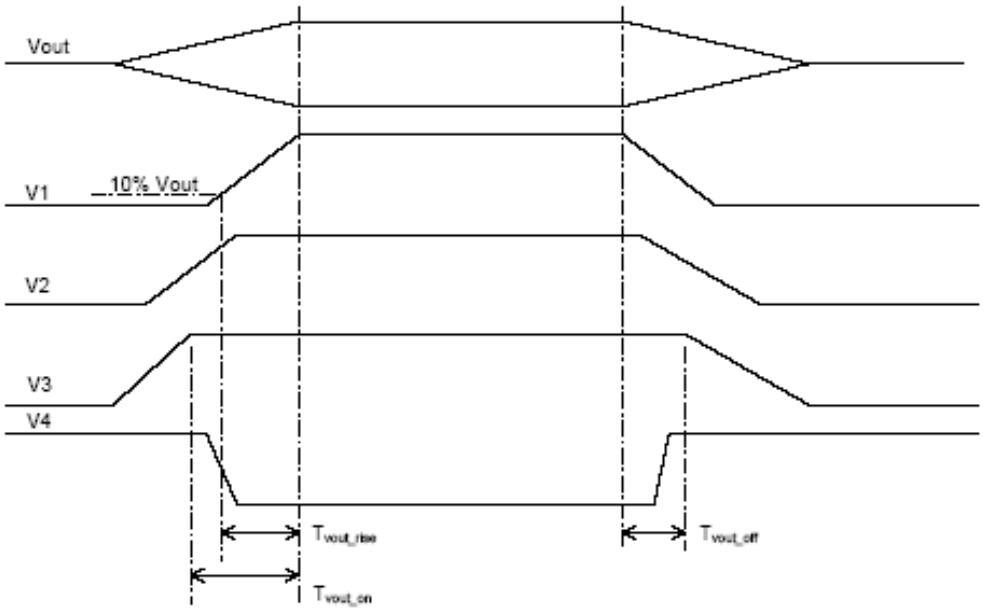


Figure 2: Output Voltage Timing

Item	Description	MIN	MAX	Units
Tsb_on_delay	Delay from AC being applied to 5 VSB being within regulation.		1500	ms
T ac_on_delay	Delay from AC being applied to all output voltages being within regulation.		2500	ms
Tvout_holdup	Time all output voltages stay within regulation after loss of AC at 75% load	17		ms
Tdc_good_hold up	Delay from loss of AC to deassertion of DC Good	16		ms
Tpson_on_dela y	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
Tpson_dc_good	Delay from PSON# deactive to DC Good being deasserted.		50	ms
Tdc_good _on	Delay from output voltages within regulation limits to DC Good asserted at turn on.	50	120	ms
Tdc_good _off	Delay from DC Good deasserted to output voltages dropping out of regulation limits.	1		ms
Tdc_good_low	Duration of DC Good being in the deasserted state during an off/on cycle using AC or the PSON# signal.	100		ms
Tsb_vout	Delay from 5 VSB being in regulation to O/Ps being in regulation at AC turn on.	50	1000	ms
T_{sb_holdup}	Time 5VSB output voltage stays within regulation after loss of AC.	70		ms
Tsb_Vout_ri se	The rising time for +5VSB start up to be in regulation	1	25	ms
T12_Vout_ri se	The rising time for +12V start up to be in regulation or rising slope 1V/ms	5	20	ms

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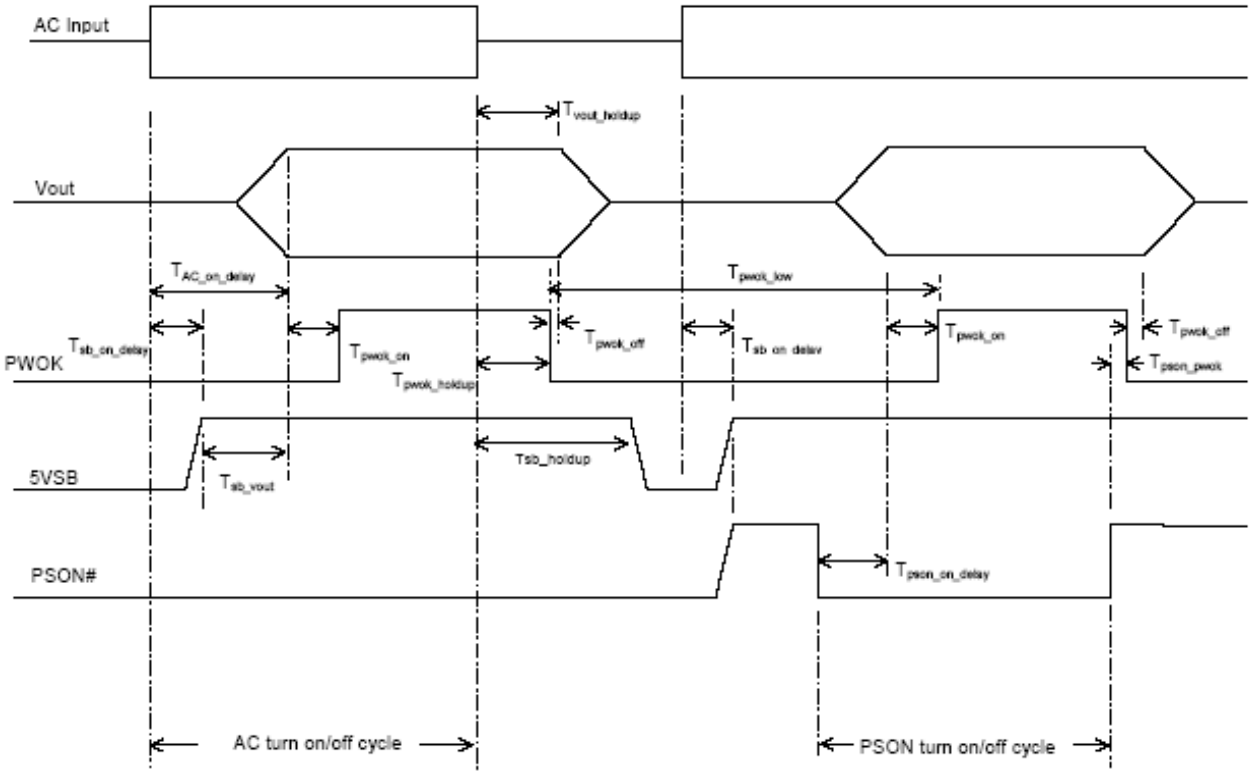

Figure 3: Turn On/Off Timing

8.1 Output sequencing

The power supply shall be turned-on by one of two ways:
With AC already applied, by driving the "**On/off#**" input signal to a low state. When the "**On/off#**" signal is transitioned to LOW state, the output must be in regulation within 400 ms maximum and the LED shall be lit with green color if the power supply is operating normally.
By applying AC to the primary input, with the "**On/off#**" input signal tied to a low state. With this method, the output must be in regulation within 2500ms and the LED shall be lit with green color if the power supply is operating normally.
When AC power is applied to the power supply, LED on the front panel of the power supply shall be illuminated with amber color.

8.2 Standby Sequencing

5Vsb shall be on (high) whenever AC Voltage is within the input range specified in "**AC Input**".

8.3 Auto Restart

The power supply shall be capable of automatically restarting due to a temporary AC outage. When AC returns, it is assumed to be within the operating range defined in section "**AC Input**".

8.4 Reset After Shutdown

When the power supply latches into shutdown either due to an internal power limit condition or due to a fault on an output (over current or short circuit), it shall return to normal operation only after the fault has been removed and the power supply is reset. Reset can be accomplished in one of two ways:
By toggling the "**ON/OFF#**" signal from low-to-high-to-low. The duration of the 1st low time necessary to reset the power supply must be no longer than 100 msec.
By removing primary power. AC must be removed for at least one second before reapplying.

8.5 Power Supply Behavior When Faulted

A faulted power supply shall not sink more than 100 ma current from the 12V output. The I2C bus status shall be operational and valid.
A power supply that fails due to an Over-Voltage condition will shutdown gracefully and will not cause shutdown of other power supplies in parallel. Standby supply will remain on.

9. Controls and Monitoring

9.1 Signal Requirements

All output logic signals will be open collector and 5V compatible except I2C signals (clock and data) which are 3.3V compatible. The power supply will sink less than 1uA as a logic high and sink at least 20 mA as a logic low. A logic low must be less than 0.4V while sinking 20mA. Signal transitions, with a 10K Ohm resistor pulling the output to 3.3/5.0V, must be clean (glitch free) and bounce free. The rise/fall time can be no slower than 5usec, measured at 10% and 90% points. The power supply will pull each logic input up to 3.3V with a resistor whose value is between 10K Ohm and 50K Ohm and provide a 100pF ceramic capacitor, signal to ground. The power supply will accept 0.8V or less as a logic low and 2V or greater as a logic high. There will be a 300mV, minimum hysteresis between a logic low and a logic high. The host will be able to sink 0.5 mA for a logic low. I2C clock and data signal shall meet 3.3V logic high and low. I2C clock and data signal line shall not add capacitor. I2C clock bus frequency is about 10 KHz, and signal rise/fall time at 5μs to 300ns shall not affect I2C functions.

9.2 Direct Signals

These signals are wired directly from the power supply to the system, which are shown on pin assignment diagram.

9.3 On/Off#

The **ON/OFF#**" signal is an active low input used to activate the power supply 12 output voltage. If AC input is already applied, the 12V output shall be within regulation no less than 100ms after **ON/OFF#** is pulled low. When this signal is HIGH the power supply must remain off.

9.4 DC Good

The power supply shall provide an output signal, "**DC GOOD**", which indicates that the 12V output is within the OV/UV limits.

Note: The "**DC GOOD**" signal shall be terminated at near of the output power supply connector with a 0.01 uF ceramic capacitor to filter out unwanted noise voltage.

9.4.1 Status during Over-temperature

When the power supply maximum temperature is exceeded, the "**DC GOOD**" signal must go LOW at least 5ms before 12.2V output is removed.

9.4.2 Status during DC Turnoff and AC Outage

When the **ON/OFF#** signal is cycled HIGH, the "**DC GOOD**" signal shall go LOW a minimum of 1 ms prior to 12V dropping out of regulation as described in section "**DC output regulation**". DC GOOD signal shall remain HIGH for at least 17 ms after AC power is removed and shall go LOW at least 1 ms before any output voltage falls below the regulation limits described in "**DC Output regulation**".

9.4.3 Status during PLD

DC GOOD signal shall remain HIGH during the "error free" part of Power Line Disturbances (PLDs) defined in section "**Power Line Disturbances (PLD) Requirements**".

9.5 Present Detect#

The "**Present Detect#**" signal shall be pulled HIGH by the system. This signal pin is hard wired to ground in the power supply and alerts the system whenever a power supply is inserted into the slot.

9.6 Ishare

This is an analog signal that is used to insure current sharing of the 12V output between two power supplies. It also represents the amount of the loading on the power supply (or supplies). It is noted that, with two power supplies sharing current, the percentage is the combined current for two power supplies, not one. The Host system may use this signal to monitor power supply loading.

Ishare Voltage	
% of max. current capacity	Voltage level (+/- 10%)
25%	2V
50%	4V
100%	8V

9.7 Remote Voltage Sense (+ & -)

The remote voltage sense signal is used to keep the 12V output voltage within regulation at load. In an event of the sense line is shorted to DC return, 12V output shall be latch off.

10. Standby Voltage requirement

10.1 Standby output voltage diode/FET Or'ing

The power supply shall have ORing diode/FET that allows the 5Vsb to be connected in parallel with another 5Vsb power supply. If an internal fault occurs on the primary circuits, the

internal logic of the power supply I2C will continue to operate from the OR'ed 5Vsb of the unit operating in parallel.

10.2 Standby Current Sharing

5Vsb is not required to share current.

10.3 Standby supply stability

5Vsb shall be unconditionally stable under all system load and AC line conditions while operating alone or in parallel with one or more power supplies.

10.4 Standby Over voltage Protection

The power supply will shut down if 5Vsb on the anode side, exceeds 6V plus the ORing diode voltage drop. The protection circuitry must be independent from the regulation circuitry including voltage references and secondary-primary feedback elements. No single component failure may cause a sustained over voltage.
Note: A shutdown caused by an over voltage in one power supply will not cause the other power supply in parallel to shutdown.

10.5 Standby Current Limit Protection

The 5Vsb current limit threshold is defined in specification table. Refer to section "Output over current protection" for detailed description.

11. Redundancy/ N+N Operation

11.1 Current Sharing Operation

The power supply shall be designed for active current sharing.
Two power supplies will be paralleled in a system. Each power supply must be able to share load to within +/- 10% share error measured 25, 50, 100% of single power supply full load current.
5Vsb requires an "ORing" diode to provide protection against internal short circuit fault.

11.2 Output Isolation Oring MOSFET

The 12V output current must pass through an Oring MOSFET to protect the bus voltage against a power supply internal fault.

11.3 Power Supply Behavior When Faulted

- The faulted supply shall not sink more than 100 ma current.
- I2C bus status shall be operational and valid, refer to "**I2C Bus/VPD Interface**".
- The "DC Good" signal and "DC Good Fault" bit status shall be valid.
- A power supply that fails due to a 12V or 5Vsb Over-Voltage condition will shutdown gracefully and will not cause shutdown of the other power supplies in parallel.

11.4 Parallel operation stability

The power supply shall exhibit stable operation under no/full load, full input voltage range and overall operating temperature conditions when operated in parallel.

11.5 Hot Swap Operation

The power supply must be designed with “hot swap” function with or without active AC line cord. After Hot swap I2C address shall be same as host power supply backplane hardware assigned. Host existing working power supply shall not be affected by hot swapping power supply.

12. Light Emitting Diodes (LED)

All LEDs shall protrude beyond the supply chassis surface for improved visibility**.** A single 2 color (green/amber) LED will be used in this power supply.

12.1 DC Good LED Indicator

A green/amber double color Light Emitting Diode (LED) shall be mounted as indicated in mechanical drawing and shall indicate the status of the DC GOOD signal with green color. The LED shall continue to glow under normal operation of the power supply. If this LED is not lit the power supply is **not** operating properly.

12.2 AC/5Vsb Good LED Indicator

The green/amber Light Emitting Diode (LED) shall be mounted as indicated in mechanical drawing and shall indicate the status of the 5Vsb within regulation range,12V is off and the AC line voltage is within the operating range of the power supply. The LED will show a status of amber under this condition.

13. Power Supply Compliance Agency and Environmental Requirements

13.1 Safety and EMI

Regulatory Certification/Compliance Plan			
Item	**Certification**	**Required Country**	**Acceptable Markings**
1	Product Safety Compliance/Certification		
1.1	UL60950	US	c UL us or UL
1.2	CSA 60950	Canada	c UL us or CSA
1.3	EN60950	Europe	
1.4	IEC60950 and National Deviations	International	none
1.5	Nordics – EMKO-TSE (74-SEC) 207/94	Denmark, Iceland,Finland, Narway, Sweden	none
1.6	GS Marking(Geprüfte Sicherheit, meaning Safety Tested)	Germany	none
1.7	Bauart Marking	Germany	TÜV Rheinland Product Safety; BAUART GEPRÜFT TYPE APPROVED
1.8	CE Marking: Low Voltage Directive 73/23/EEE	Europe	none
1.9	GB4943- CNCA Certification (“GB=Guo Biao”, means “National Standard”).	China	CCC
1.10	BSMI – Safety Certification (Safety, EMC)	Taiwan	none
1.11	CB Reporting with applicable deviations	Nationals	none
2	Product EMC Compliance/Certification		
2.1	FCC part 15	USA	none
2.2	ICES-003 - Emissions	Canada	none
2.3	CISPR 22 – Emissions	International	none
2.4	EN55022 - Emissions	Europe	none
2.5	EN61000-3-2 - Harmonics	Europe	none
2.6	EN61000-3-3 - Voltage Flicker	Europe	none
2.7	CE – EMC Directive 89/336/EEC	Europe	none
2.8	JEIDA (CISPR 22)	Japan	none
2.9	AS/NZS 3548 Emissions (AS/NZS CISPR 22:2002)	Australia / New Zealand	none
2.10	BSMI CNS13438 Emissions	Taiwan	none
2.11	GB 9254 – (EMC) Certification	China	none
2.12	GB 17625 - (Harmonics) CNCA Certification	China	none
2.13	EN55024 - Immunity (Europe)**		
	a) EN61000-4-2 Electrostatic Discharge	Europe	none
	b) EN61000-4-3 Radiated RFI Immunity	Europe	none
	c) EN61000-4-4 Electrical Fast Transients	Europe	none
	d) EN61000-4-5 Electrical Surge	Europe	none
	e) EN61000-4-6 RF Conducted	Europe	none
	f) EN61000-4-8 Power Frequency Magnetic Fields	Europe	none
	g) EN61000-4-11 Voltage Dips and Interruptions	Europe	none

13.2 ROHS Compliance

The unit shall comply with DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment. The 2010 lead exemption will be applicable to this unit.

13.3 Humidity

Operating: up to 90% non-condensing.
Non-operating: up to 100% (but excluding rain) during shipment. up to 95% non-condensing once installed in a system.

13.4 Altitude

Operating: up to 10,000 feet.
Non-operating: up to 35,000 feet
.

13.5 Temperature:

Operating: -5 to 50 degree Celsius.
Non-operating: -40 to 70 degree Celsius.

13.6 Power Line Disturbance Requirements

Unit shall comply with the following requirements;

EU Reference	Title of Standard	International Reference	Test Level Heavy Industrial
EN 61000-4-5	Electromagnetic Compatibility (EMC) – Part 4: -- Section 5: Surge Immunity Test	IEC 1000-4-5	1, 2kV differential 2, 4kV common
EN 61000-4-4	Electromagnetic Compatibility (EMC) – Part 4: -- Section 4: Electrical fast transient/burst immunity test	IEC 1000-4-4	1, 2, 4kV - Power 0.5, 1, and 2kV - Signal

13.7 Reliability

The MTBF data shall be presented in couple of methods, 1) a calculation method that will have a minimum MTBF at continuous operation of 100,000 hours at nominal input voltage (110/240Vac), 75% load in an ambient of 35°C, 2) a demonstrated method that will have a minimum of 250,000 hours under similar operating condition. The calculation shall be made in accordance to Bellcore RPP.

14. I^2C protocols to meet Super Micro standard.

14.1 I^2C/PSMI Bus/VPD interface

Power supply shall comply with the necessary sections of the Intel Power Supply Management Interface(PSMI) Design Guide Revision 2.12 and IPMI Platform


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14.2 Supermicro memory map requirements

Slave address will be 0x70 (default), 0x72, 0x74, 0x76
All the data follows FRU spec.

There is an Internal Area in FRU that is used and defined by
vendor (us). Therefore, we use it for health monitoring.
It is located in second block (offset 0x08),
Offset 0x09: Internal Temperature, hottest spot inside the power supply
Offset 0x0A: Fan 1 speed, RPM in the power supply
Offset 0x0B: Fan 2 speed, RPM in the power supply
Offset 0x0C: Power Status, Value to represent DC GOOD status
Offset 0x0D: Temperature High Limit, Value is fixed and is the highest acceptable internal temperature that the power supply can sustain (see Table 3).
Offset 0x0E: Fan 1 speed Low Limit, is fixed and should be the lowest fan RPM of 5954.
Offset 0x0F: Fan 2 speed Low Limit. is fixed and should be the lowest fan RPM of 5954
Offset 0x10-0x17: reserved for future use.

Power Status: bit0 =1 -> GOOD, bit0 = 0 -> Failed
Fan Speed formula: RPM=(1/0.262) *(Fan Pulse Count * 60 /2)

If user wants to retrieve the FRU data, they must follow FRU spec.
Power supply I2C operation shall not latch the system, I2C bus for over certain time period needed for normal operation. Power supply I2C shall have auto reset function in case of waiting for clock pulse over a reasonable time period.

A delay of 30 seconds from the time that DC good goes high, shall be incorporated in to the firmware before the I2C address lines are read and applied to the power supply. The bus should be inactive during this 30 sec period.

The EEPROM for the FRU data will have a minimum of 100 read/write cycles.

The CLK and DATA lines will be pulled up internally to 3.3V with two separate 2K ohm resistors.

15. Shock and Vibration

15.1 Vibration

Power supply should withstand a non-operational: Sinusoidal vibration, 1.0 G acceleration. 3-200Hz, sweep at 1/2 octave/min from low to high frequency, and then from high to low. Thirty minute dwell at all resonant points, where resonance is defined as those exciting frequencies at which the device under test experiences excursions two times larger than non-resonant excursions.
Plane of vibration to be along three mutually perpendicular

15.2 Mechanical Shock

The power supply will withstand the following imposed conditions without electrical or mechanical failure:
Non-operating Square Wave Shock: 40G, square wave at 200in/sec;on all six sides.
Non-operating half sine shock: Half Sine pulse for 70in/sec for 2ms; on all sides except top.
Operating half sine shock: Half Sine pulse for 40in/sec for 2ms; on all sides except top.

16. Mechanical Requirements

16.1 Outline Drawing

See drawing pdf included below.

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16.2 Fan Speed Control

The power supply will have two internally controlled 28mm fan. The fan will be 4 wires PWM Fan controlled by internal temperature and will have a slope of TBD.

16.3 Output Connector

The power supply will be fitted with powerblade FCI connector part no 51720-0601603AB type or equivalent. The connector includes 3 power pins for AC input, 14 signal pins and 6 power pins for 12V and return. See power supply mechanical drawing for dimensions.

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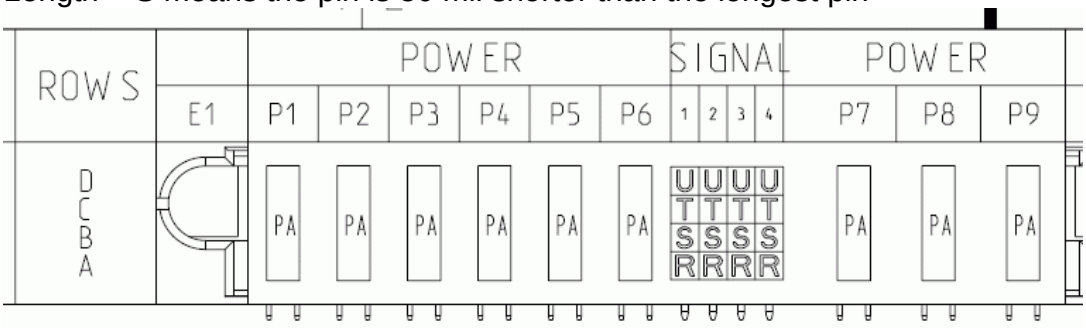
Power and Signal Connection

Pin #	Length	*Description / NET*	I/O
P1		+12Vo	analog O/P
P2		+12Vo	analog O/P
P3		+12Vo	analog O/P
P4		GND	analog O/P

P5		GND	analog O/P
P6		GND	analog O/P
D1	S	-RS (remote sense)	analog I/P
D2		+5Vsb	analog O/P
D3		+5Vsb	analog O/P
D4		+5Vsb (optional, must be open if not used)	analog O/P
C1		SCL	digital
C2		SDA	digital
C3		SIGNAL_GND (optional, must be open if not used)	digital
C4	S	PS_ON	TTL I/P
B1		+12V DC_GOOD (early warning)	O/P
B2	S	I_SHARE	analog O/P
B3	S	+RS (remote sense)	analog I/P
B4			
A1		A0	digital
A2		A1	digital
A3		PRESENT	TTL O/P
A4		Reserved for power supply vendor	
P7		EARTH	Chassis GND
P8		NEUTRAL	power I/P
P9		LINE	power I/P

Length = S means the pin is 50 mil shorter than the longest pin



Barcode: P1K43CYWWRMSSSS.

16.4 Product Labeling and Bar coding Requirements

Supermicro requires that the unit serial number be on both the power supply and matching outside carton/packaging.

16.5 Product Shipment Packaging

The power supply shipping package shall be design to provide protection from the environmental conditions it will be exposed from the manufacturing site to the final customer. The packaging shall be configured in a way that power supply can be individually packaged and shipped via normal parcel delivery or packaged in palletized format for high volume

production shipment. The packaging shall comply with International Safe Transit Association (ISTA) procedures 3D and 3E.

16.6 Compatibility

No safety issue (Cross Fire) occurred when Swap in the redundant system with competitor PSU.

17. outside mechanical drawing