Compuware Technology Inc.

Power Supply Hardware Specification

Model: CDR-2721-2M1

Revision Histories

Rev.	Description	Issued Date	Released by
P1	Draft spec.	5/2/2023	Jack Cheng
P2	Spec. Released	11/10/2023	Jack Cheng

Specification is subject to change without notice

Approved by: **Checked by:** **Prepared by:**

1. Introduction

This specification defines the performance characteristics of a single-phase (3-wire), digital 2700W redundant, single output power supply with wide range input AC capability (180-264VAC/47-63Hz), HVDC (180-300Vdc) and Titanium level. The power supply shall be designed for parallel operation and with DSP controllers. In the event of a power supply failure, the redundant power supply continues to power the system even under over voltage fault. The number of power supplies per system will be limited to a maximum of four. The power supply shall be designed for “hot swap” exchange and must contain the OR-ing isolation MOSFETs for all outputs and shall communicate to external devices through Inter-Integrated (I2C) Circuit protocol. The power supply will have an EEPROM for storing powers supply FRU information, and meet PMBus Revision 1.2 requirement. This product follows the CRPS-185 specification.

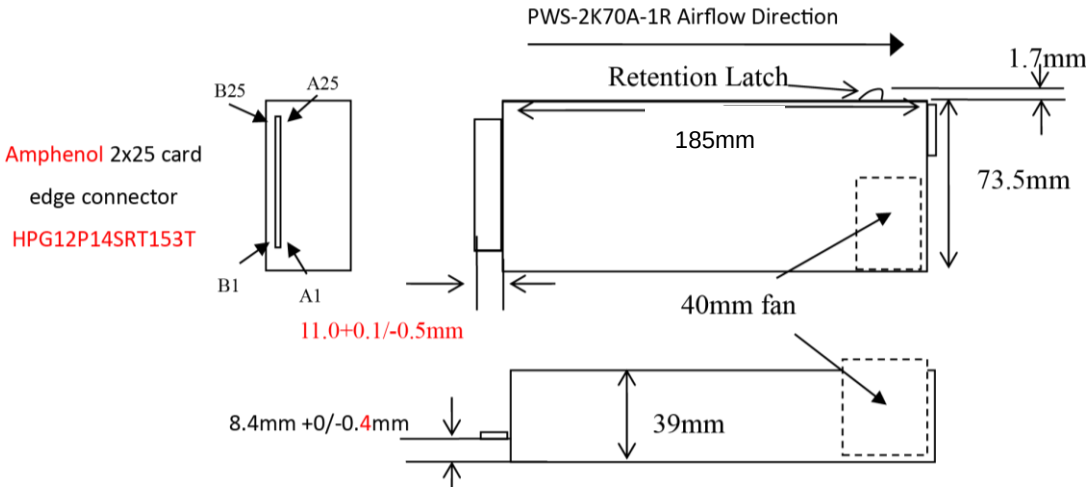
1.1. Design and Assembly Standard

This model is designed to be long life product with expected life time of 5 years of operation following and meet IPC9592B Class I stress factor de-rating requirements and with at least 5 years life and endurance, and quality control criteria should be based on IPC- A-610 class 2. All units shipped should meet IPC-A-610 class 2 guideline for assembly quality acceptance.

The assembly process should follow IPC-J-STD-075, IPC-J-STD-001, IPC-J-STD-003, IPC-7711A/7721A, IPC-HDBK-830, and other IPC, and J-STD for general production practice. All cable and wire harness assemblies should meet IPC-A-620 class II requirements. Printed boards should meet IPC-A-600 class II requirements.

2. Mechanical Overview

The physical size of the power supply enclosure is 39/40mm x 73.5mm x 185mm. The power supply contains a 40x40x28mm fan. The power supply ha es with a 2x25 card edge connector in the system. The AC plugs directly into the external face of the power supply. Refer to the following Figure 1. All dimensions are nominal. Below are for reference outline only. Refer to 2D/3D drawing for detail drawing and tolerance.



2.1. DC Output Connector

The power supply shall use a card edge output connection for power and signal that is compatible with a 2x25 Power Card Edge connector.

The power supply edge card's pinout is defined in the next table. This card edge is compatible with the higher current connectors from Amphenol* HPG12P14SRT153T. The pin map is shown in next table.

Name	High power conn 1	Regular Conn 2		Regular conn 2	High power conn 1	Name
GND	P1	A1		B1	P7	GND
GND		A2		B2		GND
GND		A3		B3		GND
GND	P2	A4		B4	P8	GND
GND		A5		B5		GND
GND		A6		B6		GND
GND	P3	A7		B7	P9	GND
GND		A8		B8		GND
GND		A9		B9		GND
+12V	P4	A10		B10	P10	+12V
+12V		A11		B11		+12V
+12V		A12		B12		+12V
+12V	P5	A13		B13	P11	+12V
+12V		A14		B14		+12V
+12V		A15		B15		+12V
+12V	P6	A16		B16	P12	+12V
+12V		A17		B17		+12V
+12V		A18		B18		+12V
PMBus SDA	S1	A19		B19	S8	A0 (SMBus address)
PMBus SCL	S2	A20		B20	S9	A1 (SMBus address)
PSON#	S3	A21		B21	S10	+12Vstby
SMBAlert#	S4	A22		B22	S11	Cold Redundancy Bus
Return sense	S5	A23		B23	S12	12V load share bus (Vshare)
+12V Remote sense	S6	A24		B24	S13	Present (connect to ground)
PWOK	S7	A25		B25	S14	No connect

1. High power connector Amphenol model HPG12P14SRT153T
2. Regular 50-pin card edge connector FCI-Amphenol model 10035388-102LF. (not used for this model)

2.2. Handle Retention

The power supply shall have a handle to assist extraction. The module should be able to be inserted and extracted without the assistance of tools. The power supply should have a latch which retains the power supply into the system and prevents the power supply from being inserted or extracted from the system when the AC power cord is pulled into the power supply. The handle should protect the operator from any burn hazard.

2.3. LED Marking and Identification

The power supply shall use a bi-color LED; Amber and Green. Below are tables showing the LED states for each power supply operating state and the LED's wavelength characteristics. An example of bi-color LED that meets the below characteristics is Kingbright* WP59-CN99.

Table 2-1 LED Characteristics

	Min λd Wavelength	Nominal λd Wavelength	Max λd Wavelength	Units
Green	562	565	568	nm
Amber	607	610	613	nm

Table 2-2 LED Definition

Power Supply Condition	LED State
Output ON and OK	GREEN
No AC power to all power supplies	OFF
PSU standby state AC present / Only 12VSB on	1 Hz Blink GREEN
Power supply is cold standby state or always standby state as defined in the Cold Redundancy section of the CRPS Common Requirements Specification	1 Hz Blink GREEN
AC cord unplugged, or AC power lost; with a second power supply in parallel still with AC input power.	AMBER
Power supply critical event causing a shutdown; failure, over current, short circuit, over voltage, fan failure, over temperature	AMBER
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1 Hz Blink Amber
Power Supply Firmware updating	2 Hz Blink Green

2.4. Acoustic Requirements

The power supply should incorporate variable speed fan(s). The declared sound power levels (LwAd) of the power supply must meet the requirements shown in the table below. Sound power must be measured according to ECMA* 74 (www.ecma-international.org) and reported according to ISO 9296/ISO7779. The sound pressure measurement must be measured from a distance of 1m from the face of the fan, centered on the AC connector face of the power supply. The sound power measurement is optional, and the sound pressure measurement is required.

Table 2-3 Sound Power Requirement

Inlet Temperature Condition	% of Maximum Loading Condition	Altitude	Sound Power (BA)	Sound Pressure (dBA)
50 °C	80%	900m	9.0	80
40 °C	45%	900m	8.0	70
35 °C	20%	900m	7.0	60

2.5. Temperature and Altitude Requirements

The power supply shall operate within all specified limits over the T_{op} temperature range. All airflow shall pass through the power supply and not over the exterior surface of the power supply.

Table 2-4 Environmental Requirements

ITEM	DESCRIPTION	MIN	MAX	UNITS
T_{op}	Operating temperature range (100% loading)	0	55	°C
$T_{op\_redundant}$	Operating temperature range (60% loading)	0	60	°C
$T_{non\text{-}op}$	Non-operating temperature range	-40	70	°C
T_{exit}	Maximum exit air temperature		68	°C
Altitude	Maximum operating altitude		5000	Meter

Note: Under normal conditions, the exit air temperature shall be less than 65 °C. 68 °C is provided for absolute worst case conditions and is expected only to exist when the inlet ambient reaches 55 °C. The system level fan speed control shall be able to influence the system fans and power supply fans to increase fan speeds, as necessary, to maintain cooling up to 14 CFM total flow.

The power supply must meet UL enclosure requirement for temperature rise limits. All sides of the power supply with exception to the air exhaust side must be classified as “Handle, knobs, grips, etc. held for short periods of time only.”

2.6. Airflow Requirements

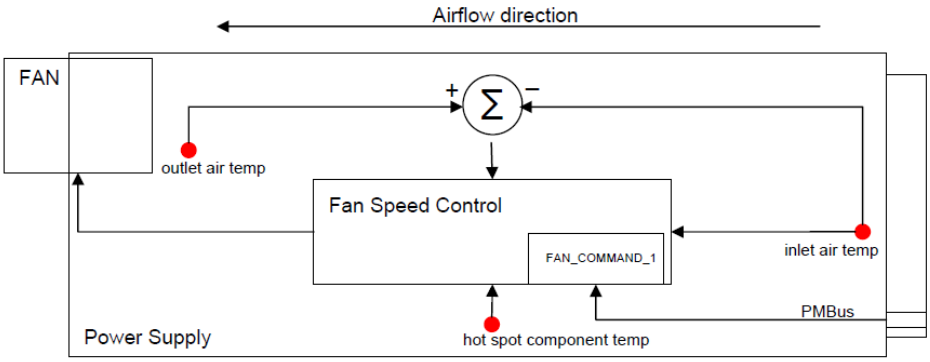
The power supply shall incorporate a 40X28mm fan for self cooling in system with higher airflow impedances. The airflow direction shall be from the card edge connector side to the AC inlet side of the power supply.

The fan speed control must have close loop algorithm based on the critical component temperature and the ambient temperature (inlet temperature). Thus, ensuring the PSU fan will always ramp to maximum speed under any condition to protect the power supply from overheating. These conditions include high ambient temperatures, loading, AC input, and airflow impedance.

Under any steady state operating condition (steady state power output level and steady state inlet air temperature), fan oscillation shall be controlled such that associated sound power level variation falls within a band of 2.0 dBA (roughly 10% mean speed). This condition may be treated as steady state fan speed condition.

After the new load and/or cooling condition steady state is established, transition to the steady state fan speed shall take place within 60s.

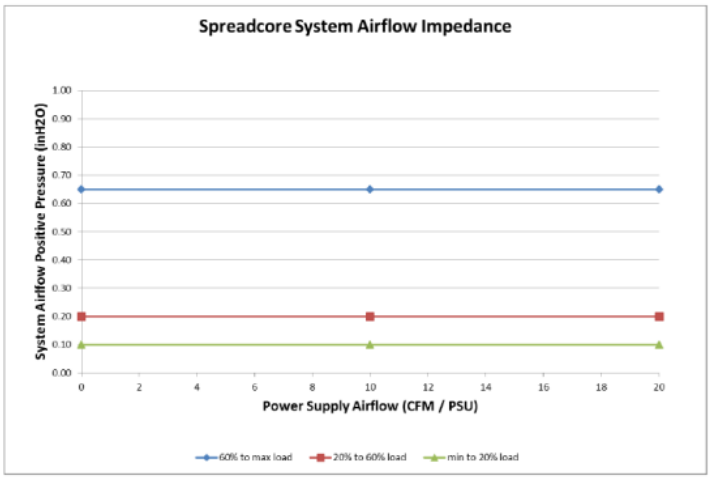
Figure 2-1 Power Supply Fan Speed Control Block Diagram for CDR-2721-2M1



The power supply shall be able to cool itself with the following system airflow impedance curves defining the pressure versus flow characteristics the power supply will see when installed in a system. The three curves correlate to the acoustic operating states of idle, operating, and performance. The test condition for these cases is 200VAC and maximum junctions temperature are 120°C for reliability requirements. The power supply still needs to meet safety requirement for testing at 180VAC at all these conditions.

During standby mode, the fan should run at minimum fan speed. As inlet temperature or 12Vsb loading increase, the fan speed may increase to improve the cooling.

Figure 2-2 Spreadcore System Flow Impedance



2.7. Minimal PSU Fan Speed

In some system applications, there is a possibility that the airflow through the PSU will reverse direction and lead to component exceeding their thermal limits. To prevent this reverse airflow condition, the PSU must support the PMBus command to boost th e PSU fan speed. System will communicate the minimal fan speed to the PSU via the FAN_COMMAND_1 (3Bh) PMBus command. This sets the PSU minimum fan speed to guarantee positive airflow direction through the PSU.

2.8. Thermal Sensors, CLST, and OTP

The PSU shall have thermal sensors to measure inlet temperature and hot spot component temperature(s). These shall be used for asserting Over Temperature Warning condition (OTW), Over Temperature Protection/shutdown (OTP), reporting temperatures via PMBus, and for controlling the fan speed.
Thermal sensors accuracy shall be within +/-2 °C.

The hotspot thermal sensor(s) shall have both OTW level and OTP level associated with them. The OTW level must be set at least 4°C lower than the OTP level to guarantee a warning condition is reported to the system before a shutdown condition. OTW: Over temperature warning level associated with all thermal sensors. This asserts the SMBAlert# signal and does not shutd own the PSU. This also asserts the associated PMBus STATUS warning bits. This support the CLST (Closed Loop System Throttling) feature.

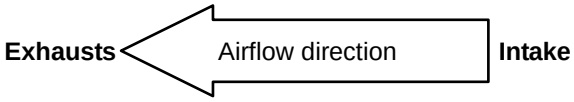
OTP: Over temperature protection level associated with all thermal sensors. This shuts down the PSU to protect any components from exceeding their maximum temperature. This also asserts the associate PMBus STATUS bits.
Inlet Ambient Sensor Trip level

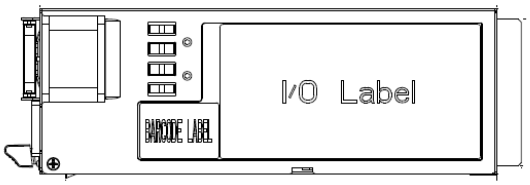
	Min.	Nominal (firmware setting)	Max.
Over temp warning; inlet air (OTW)	N/A (based on hotspot only)	N/A (based on hotspot only)	N/A (based on hotspot only)
Over temp shutdown; inlet air (OTP)	N/A (based on hotspot only)	N/A (based on hotspot only)	N/A (based on hotspot only)

Note: Internal fan speed control algorithm shall ramp up the fan speed to the maximum prior to the SMBAlert insertion.

2.9. Airflow direction

CDR-2721-2M1 air direction is





3. AC Input Requirements

3.1. AC Inlet Connector

The AC input connector shall be an IEC 320 C-20 power inlet. This inlet is rated for 16A / 250VAC.

3.2. AC Input Voltage Specification

The power supply must operate within all specified limits over the following input voltage range. Harmonic distortion of up to 10% of the rated line voltage must not cause the power supply to go out of specified limits. Application of an input

voltage below rated VAC shall not cause damage to the power supply, including a blown fuse.

Table 3-1 AC Input Voltage Range

PARAMETER	MIN	RATED	V_{max}	Start up VAC	Power Off Vac
AC Voltage (highline)	180 V_{rms}	200-240 V_{rms}	264 V_{rms}	175-179Vac	160-175Vac
Frequency	47 Hz	50/60	63 Hz		
DC Voltage	180Vdc	240 Vdc	300Vdc	166-179Vdc	150-165Vdc

Notes:

1. Maximum input current at high input voltage range shall be measured at 180VAC, at max load.
2. This requirement is not to be used for determining agency input current markings.
3. The Power supply must have the DC input OVP & UVP functions and will be auto-recovered after applying correct DC input voltage.
4. The OVP setting point is DC 305V and the UVP setting point is DC 150-165V (after start up).
5. With DC input, the power supply must work normally when the DC input positive terminal is connected to the either pole, AC “Line L” or AC “Neutral N”, of the inlet connector.
6. For CQC compliance testing, the DC input will be tested at range 180-300Vdc for +25%/-25% tolerance

3.2.1.240VDC Input Specification (China Certificate only)

The power supply must be able to operate normally with 240VDC input.

- Operating range: 180VDC to 300VDC
- PMBus commands must function normally.
- Power timing requirements met during power cycling
- Output power requirements support for same equivalent RMS AC input voltage
- LED functioning correctly
- In Always Standby mode in a 1+1 PSU configuration the active PSU will have >95 % load, the Standby PSU will have <5 % load
- In 1+1 PSU configuration and one PSU Active and the other in Always Standby mode; if the Active PSU fails the Standby PSU m ust support the load to maintain output voltage > 11.20V. Tested with 2,200 uF 12V capacitance.

3.3. AC Line Isolation Requirements

The power supply shall meet all safety agency requirements for dielectric strength. Transformers’ isolation between primary and secondary windings must comply with the 3000Vac (4242Vdc) dielectric strength criteria. If the working voltage between primary and secondary dictates a higher dielectric strength test voltage the highest test voltage should be used. In addition, the insulation system must comply with reinforced insulation per safety standard IEC 950. Separation between the primary and secondary circuits, and primary to ground circuits, must comply with the IEC 950 spacing requirements.

3.4. AC Line Dropout / Holdup

An AC line dropout is defined to be when the AC input drops to 0VAC at any phase of the AC line for any length of time.

During an AC dropout the power supply must meet dynamic voltage regulation requirements. An AC line dropout of any duration shall not caus e tripping of control signals or protection circuits other than the SMBAlert# signal. If the AC dropout lasts longer than the holdup time the power supply should recover and meet all turn on requirements. The power supply shall meet the AC dropout requirement ove r rated AC voltages and frequencies. A dropout of the AC line for any duration shall not cause damage to the power supply.

Table 3-2 Holdup Time

Loading	12V Output Holdup Time	PWOK Holdup Time
0% to 70% of rated load (2700W)	At least 11.2msec	At least 10msec

Note: This must be tested with a bulk capacitor having the minimum capacitance tolerance, at worst case loading and at worst case AC voltage conditions.

3.4.1. AC Line 12VSB Holdup

The 12VSB output voltage should stay in regulation under its full load (static or dynamic) during an AC dropout of 70ms min (=12VSB holdup time) whether the power supply is in ON or OFF state (PSON asserted or de-asserted).

Table 3-3 Vsb Holdup time

Loading	12VSB Output Holdup Time	
	Min	Max
0% to 100% of rated load (2700W)	70msec	5000msec

3.5. AC Line Fuse

The power supply shall have one line fused in the single line fuse on the line (Hot) wire of the AC input. The line fusing shall be acceptable for all safety agency requirements. The input fuse shall be a fast blow type. AC inrush current shall not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply shall not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

3.6. AC Inrush

AC line inrush current shall not exceed 35A peak, for up to one-quarter of the AC cycle, after which, the input current should be no more than the specified maximum input current. The peak inrush current shall be less than the ratings of its critical components (including input fuse, bulk rectifiers, and surge limiting device).
The power supply must meet the inrush requirements for any rated AC voltage, during turn on at any phase of AC voltage, durin g a single cycle AC dropout condition as well as upon recovery after AC dropout of any duration, and over the specified temperature range (Top).

3.7. AC Line Transient Specification

AC line transient conditions shall be defined as “sag” and “surge” conditions. “Sag” conditions are also commonly referred to as “brownout”, these conditions will be defined as the AC line voltage dropping below nominal voltage conditions. “Surge” will b e defined to refer to conditions when the AC line voltage rises above nominal voltage. The power supply

shall meet the requirements under the following AC line sag and surge conditions.

Table 3-4 AC Line Sag Transient Performance

AC Line Sag (10sec interval between each sagging)				
Duration	**Sag**	**Operating AC Voltage**	**Line Frequency**	**Performance Criteria**
0 to ½ AC cycle @(0-70% loading)	95%	Nominal AC Voltage ranges	50/60Hz	No loss of function or performance
> 1 AC cycle @(0-100% loading)	>30%	Nominal AC Voltage ranges	50/60Hz	Loss of function acceptable, self recoverable

Table 3-5 AC Line Surge Transient Performance

AC Line Surge				
Duration	**Surge**	**Operating AC Voltage**	**Line Frequency**	**Performance Criteria**
Continuous	10%	Nominal AC Voltages	50/60Hz	No loss of function or performance
0 to ½ AC cycle	30%	Mid-point of nominal AC Voltages	50/60Hz	No loss of function or performance

During no load under AC transient condition, the power supply would not trip any protection (ex. OVP, UVP etc).

3.8. Susceptibility Requirements

The power supply shall meet the following electrical immunity requirements when connected to a cage with an external EMI filter which meets the criteria defined in the SSI document EPS Power Supply Specification.

Table 3-6

Level	Description
A	The apparatus shall continue to operate as intended. No degradation of performance.
B	The apparatus shall continue to operate as intended. No degradation of performance beyond spec limits.
C	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls

3.9. Electrostatic Discharge Susceptibility

The power supply shall comply with the limits defined in EN 55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-2: Edition 1.2: 2001-04 test standard and performance criteria B defined in Annex B of CISPR 24.

3.10. Fast Transient/Burst

The power supply shall comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-4: Second edition: 2004-07 test standard and performance criteria B defined in Annex B of CISPR 24.

3.11. Radiated Immunity

The power supply shall comply with the limits defined in EN55024:2010 using the EN61000-4-3: 2010 Edition 2010-04 test standard and performance criteria A defined in Annex B of CISPR 24.

3.12. Surge Immunity

The power supply shall be tested with the system for immunity to AC Unidirectional wave; 2kV line to ground and 1kV line to l ine, per EN55024:2010, EN 61000-4-5:2014

The pass criteria include: No unsafe operation is allowed under any condition; all power supply output voltage levels to stay within proper spec levels; No change in operating state or loss of data during and after the test profile; No component damage under any condition.

The power supply shall comply with the limits defined in EN55024:2010 using the EN 61000-4-5: 2014 test standard and performance criteria B defined in Annex B of CISPR 24.

Note: The power supply shall be tested to 2.6kV line to ground and 1.3kV line to line to check for design margin.

3.13. Power Recovery

The power supply shall recover automatically when the input power is restored after the lost of input power. Input power lost is defined to be any loss of input power that exceeds the dropout criteria.

3.14. Voltage Interruptions

The power supply shall comply with the limits defined in EN55024: 2010 using the EN 61000-4-11: Second Edition: 2004-03 test standard and performance criteria C defined in Annex B of CISPR 24.

3.15. Standby Circuit Fuse

The power supply standby DC to DC circuit should have an input fuse prior to the standby transformers.

4. Efficiency, iTHD, Power Factor

The following table provides the required minimum efficiency level/Power factor/Input current THD at various loading conditions. These are provided at four different load levels; 100%, 50%, 20%, and 10%. Output shall be load according to the proportional loading method defined by 80 Plus. The power supply should meet 80plus Titanium Efficiency requirements.

Table 4-1 Efficiency, PF, THD Requirement

Load (%)	Input 230Vac		
	Input current THD (%)	Power Factor	Efficiency (%)
10	Less than 25%	At least 0.9	At least 90.0
20	Less than 15%	At least 0.96	At least 94.0
40	Less than 8%	N/A	N/A
50	Less than 5%	At least 0.98	At least 96.0
100	Less than 5%	At least 0.99	At least 91.0

Note: At no load or at sleep state (200-240Vac input), the power supply should consume less than 5W with less than +/-1W instability when measured by power meter (with filtering off).

Note: During standby (PSON=off and 200-240Vac input), the power supply should consume less than 4W with less than +/-1W instability when measured by power meter (with filtering off).

Note: The power supply should pass all efficiency measurements by 0.2% to guarantee design margins for production.

5. DC Output Specification

5.1. Output Power / Current for Single PSU

The following table defines the minimum power and current ratings. The power supply must meet both static and dynamic voltage regulation requirements for all conditions.

Table 5-1 Minimum Load Rating

Parameter	Min	Rated Continuous	CLST Peak 20s Peak [2]	Pmax.app Peak 10msec Peak [3]	Pmax Peak 100µs Peak [4]
12V main (200-240VAC rating) / (240Vdc for CQC rating)	0	225 A	260A	324A	356A
12Vstby[1]	0.0	4.0A	4.5A	NA	NA

The power supply shall be stable operating at any load point from rated power up to the peak load.

Note:

1) 12Vstby must provide 6.0A with two power supplies in parallel.
2) CLST Peak load duration is based on thermal sensor and assertion of the SMBAlert# signal. Minimum peak power duration shall be 20 seconds without asserting the SMBAlert# signal at maximum operating temperature.
3) Pmax.app peak duty cycle shall be 25%; 4 ms at Pmax.app peak / 12 ms at rated current. Applying a Pmax.app peak load must not trip the SMBAlert# signal. The maximum length of time the Pmax.app peak must be supported is based on the SMBAlert# signal asserting. The PSU must support this peak load for 5 ms after SMBAlert# asserts. See Section 5.2 for details
4) Pmax peak must be support based on PMAX Protection requirements that included added system 12V capacitors. Apply loading greater than Pmax.app load may trip the SMBAlert# signal for quickly throttling the processor and memory load. See Section 5.2 for details.
5) The total max combined output follows the below table

Input Voltage	Max output combined wattage
200-240VAC / 240Vdc for CQC rating	2700W

5.2. Pmax Peak Load Protection Requirements

For peak loads above the PMax.app peak load level the PSU may assert the SMBAlert# signal to shorten the duration of the peak load to < 500 µs. For peak loads up to PMax.app peak load level the PSU must not assert SMBAert# if the peak load duration is <10 ms. If the peak load last longer than 10 ms the PSU may assert SMBAlert# to throttle the load within 15 ms. Table 5-3 are PSU requirements for PMax peak load conditions.

Table 5-2 PMAX Protection testing conditions

PSU Type	Pmax Peak Load	Peak Current	System Capacitance	SMBAlert# Timing	Peak Load Duration	Voltage Undershoot
2700W	Rated + 1572W	Rated + 131A	6 x 1,500 µF	< 20 µs	100 µs	-2%

Notes: When the peak load is applied without sufficient system capacitance, the PSU output voltage might fold back to

8.0V (b ut cannot be lower than 8V).

5.3. Standby Output

The 12VSB output shall be present when an AC input greater than the power supply turn on voltage is applied.
There should be load sharing in the standby rail. Two power supply modules should be able to support 6.0A standby current continuous.

5.4. Voltage Regulation

The power supply output voltages must stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise. These shall be measured at the output connectors.

Table 5-3 Voltage Regulation Limit

PARAMETER	TOLERANCE	MIN	NOM	MAX	UNITS
+12V	- 5% / +5%	+11.40	+12.00	+12.60	Vrms
+12VSB	- 5% / +5%	+11.40	+12.00	+12.60	Vrms

5.4.1. Output Voltage Setting point

The main 12V must be set at 12.20V+/-60mV @ 50% of rated load, and 12Vsb@0% load.
Set point voltages are measured at the fixture connector pin immediately mating with the power supply output connector (ex. Gold finger).

5.5. Dynamic Loading

The output voltages shall remain within limits specified for the step loading and capacitive loading specified in the table below. The load transient repetition rate shall be tested between 50Hz and 5kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load to the MAX load conditions.

Table 5-4 Transient Load Requirements

Output	Δ Step Load Size (See note)	Load Slew Rate	Test capacitive Load
+12VSB	1.0A	0.5 A/μsec	1000 μF
+12V	60% of max load	1 A/μsec	1000 μF

Note: For dynamic condition +12V min loading is 1A.

5.6. Capacitive Loading

The power supply shall be stable and meet all requirements with the following capacitive loading ranges.

Table 5-5 Capacitive Loading Conditions

Output	MIN	MAX	Units
+12VSB	10	3100	μF

+12V	2000	70000	μF

Note: The minimum capacitive load on 12V output is required to hold regulation during cold redundancy mode PSU failures and PSU hot swapping.

5.7. Grounding

The output ground of the pins of the power supply provides the output power return path. The output connector ground pins sha ll be connected to the safety ground (power supply enclosure). This grounding should be well designed to ensure passing the max allowed Common Mode Noise levels.

The power supply shall be provided with a reliable protective earth ground. All secondary circuits shall be connected to protective earth ground. Resistance of the ground returns to chassis shall not exceed 1.0 MΩ. This path may be used to carry DC current

5.8. Closed loop stability

The power supply shall be unconditionally stable under all line/load/transient load conditions including capacitive load ranges specified in Section 4.6. A minimum of: 45 degrees phase margin and -10dB-gain margin is required. The power supply manufacturer shall provide proof of the unit's closed-loop stability with local sensing through the submission of Bode plots. Closed-loop stability must be ensured at the maximum and minimum loads as applicable.

5.9. Residual Voltage Immunity in Standby Mode

The power supply should be immune to any residual voltage placed on its outputs (Typically a leakage voltage through the system from standby output) up to 500mV. There shall be no additional heat generated, nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also should not trip the protection circuits during turn on.

The residual voltage at the power supply outputs for no load condition shall not exceed 100mV when AC voltage is applied and the PSON# signal is de-asserted.

5.10. Common Mode Noise

The Common Mode noise on any output shall not exceed 350mV pk-pk over the frequency band of 10Hz to 20MHz. The measurement shall be made across a 100Ω resistor between each of DC outputs, including ground at the DC power connector and chassis ground (power subsystem enclosure). The test set-up shall use a FET probe such as Tektronix model P6046 or equivalent.

5.11. Soft Starting

The Power Supply shall contain control circuit which provides monotonic soft start for its outputs without overstress of the AC line or any power supply components at any specified AC line or load conditions.

5.12. Zero Load Stability Requirements

When the power subsystem operates in a no load condition, it does not need to meet the output regulation specification, but it must operate without any tripping of over-voltage or other fault circuitry. When the power subsystem is subsequently loaded, it must begin to regulate and source current without fault.

5.13. Hot Swap Requirements

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system is operating under static, dynamic, and zero loading conditions. The power supply shall use a latching mechanism to prevent insertion and extraction of the power supply when the AC power cord is inserted into the power supply.

5.14. Forced Load Sharing

The +12V output will have active load sharing. The output will share within 50% tolerance when the output loading is above 50W to 5% loading. The output will share within 10% tolerance when the output loading is above 5%. The failure of a power supply should not affect the load sharing or output voltages of the other supplies still operating. The supplies must be able to loa d share in parallel and operate in a hot-swap / redundant 1+1, 2+1, 2+2, 2+0 and 3+1 configurations. The 12VSB output is required to have passive sharing between power supplies. The 12VSB output of the power supplies are connected together in the system so that a failure or hot swap of a redundant power supply does not cause these outputs to go out of regulation in the system.

5.15. Ripple / Noise

The maximum allowed ripple/noise output of the power supply is defined in Table 14: Ripples and Noise below. This is measured over a bandwidth of 10Hz to 20MHz at the power supply output connectors. A 10μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor is placed at the point of measurement.

Table 5-6 Ripple and Noise

+12V main	+12VSB
150mVp-p	120mVp-p

The test set-up shall be as shown below.

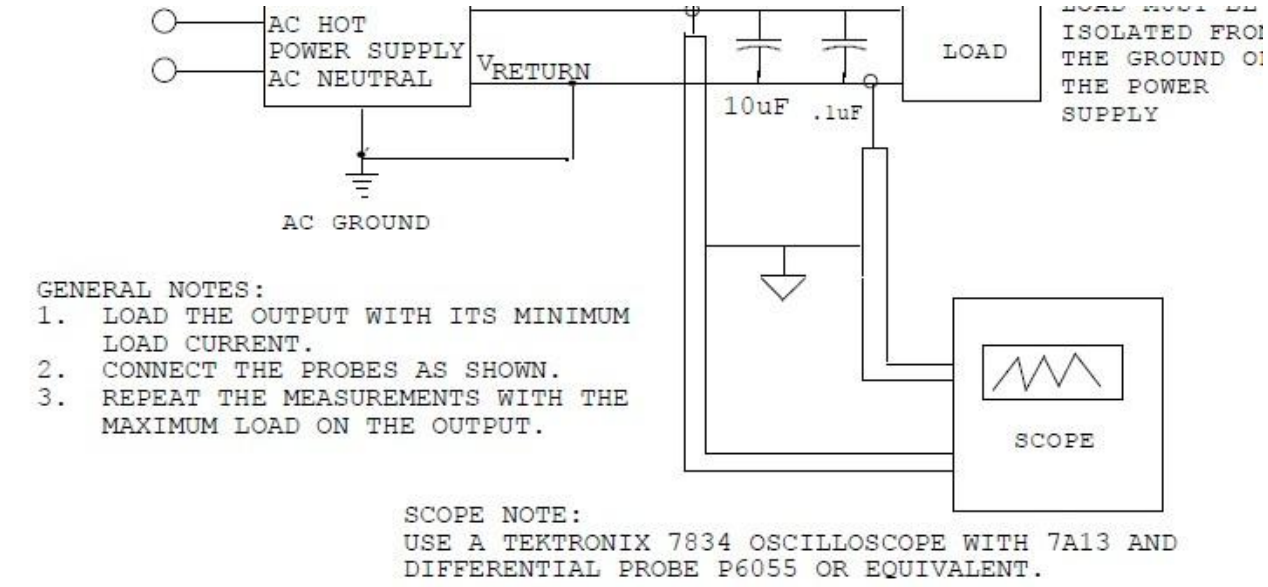


Figure 5-1 Differential Noise test setup

Note: When performing this test, the probe clips and capacitors should be located close to the load.

5.16. Timing Requirements

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (Tvout_rise) within 5 to 20ms. For 12VSB, it is allowed to rise from 1.0 to 25ms. All outputs must rise monotonically. Table below shows the timing requirements for the power supply being turned on and off via the AC input, with PSON held low and the PSON signal, with the AC input applied.

Table 5-7 Timing Requirements

ITEM	DESCRIPTION	MIN	MAX	UNITS
Tvout_rise	12V Output voltage rise time	5.0	20	ms
Toff_latch	This is the time the PSU must stay off when being powered off with loss of AC input. Both outputs must meet this OFF time; 1) whenever PWOK is de-asserted for the 12Vmain output; 2) whenever the 12Vstby output drops below regulation limits	500	1000	ms
Tvsbout_rise	12VSB Output voltage rise time	1.0	25	ms
Tsb_on_delay	Delay from AC being applied to 12VSBbeing within regulation.		1500	ms
T ac_on_delay	Delay from AC being applied to all output voltages being within regulation.		3000	ms
Tvout_holdup	Time 12V output voltage stay within regulation after loss of AC. (0-70% loading)	11.2		ms
Tpwok_holdup	Delay from loss of AC to de-assertion of PWOK (0-70% loading)	10		ms
Tpson_off_delay	Delay from PSON# de-asserted to power supply turning off		5	ms
Tpson_on_delay	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
T pson_pwok	Delay from PSON# deactivate to PWOK being de-asserted.		5	ms
Tpwok_on	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	ms

T pwok_off	Delay from PWOK de-asserted to output voltages dropping out of regulation limits.	1.2	Configura ble via PMBus	ms
Tpwok_low	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal.	100		ms
Tsb_vout	Delay from 12VSBbeing in regulation to O/Ps being in regulation at AC turn on.	50	1000	ms
T12VSB_holdup	Time the 12VSBoutput voltage stays within regulation after loss of AC.	70	5000	ms

Note: The Tpwok_holdup and Tpwok_off times are the default values in the PSU when it is being energized; however, the system now can configure the warning time stablished by Tpwok_off to have a different value,

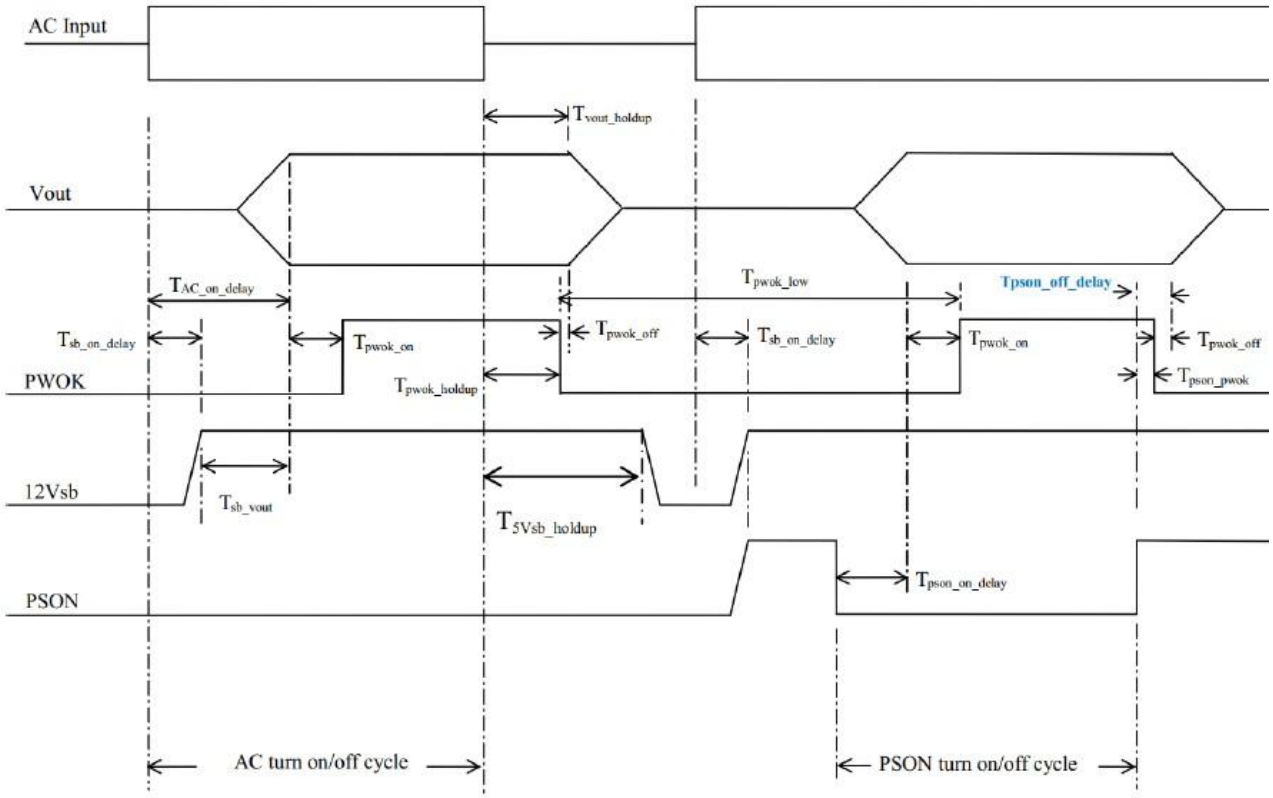


Figure 5-2 Turn on/off Timing (Power Supply Signals)

5.17. PWOK Signal Timing Requirements

The PWOK signal timing shall be as stated in *Timing requirements* when the power supply is being energized (AC/DC is applied), however the additional per-warning time established by Tpwok_off shall be configurable via PMBus command M*FR_PWOK_WARNING_TIME (F0h)* using linear format. It is recommended to use 1ms steps and the power supply shall guarantee at least the minimum warning time configured. It is recommended to have a jitter of no more than 1.5ms. Tpwok_off configurable warning time value shall return to default (0ms) after an input AC or DC cycle only. The MFR_PWOK_WARNING_TIME is adjustable between 0ms to 4ms. Any value 5ms or above will be set to the max timing 4ms.

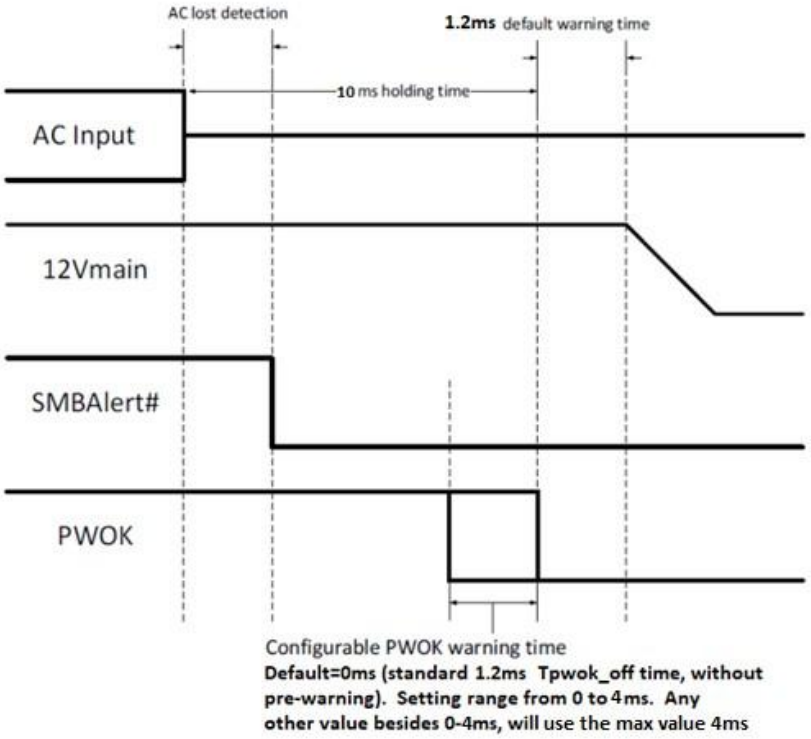


Figure 5-3

6. Protection Circuits

Protection circuits inside the power supply shall cause only the power supply's main outputs to shutdown. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 2sec and a PSON# cycle HIGH for 1sec shall be able to reset the power supply.

6.1. Current Limit (OCP)

The power supply shall have over current protection (OCP), over current warning (OCW), and over power protection (OPP) limits as defined in Table 6-1 below. These are defined to protect the PSU and to allow peak currents to power the system without the PSU shutting down.

Fast OCW and Slow OCW levels are defined to assert SMBAlert# to allow the system to throttle power to protect the PSU; but al so, to allow peak current to the system without throttling the system.

When OCP trips; it shall shutdown and latch OFF the PSU. This will be cleared only by an AC power cycle or PSON toggle. The power supply shall not be damaged from repeated power cycling in this condition.
PSON# cycling and input power cycling shall reset the over current fault/warning bit and cause the power supply to restart. 12VSB will be auto-recovered after removing OCP limit.

Table 6-1 OCP and OCW Requirements

Spec.	Description	Thresholds		Timing	
		Min.	Max.	Min.	Max.
OPP / Fast OCP 1	Over power protection (voltage foldback then latch after MIN timing)	371A	381A	100 µs	NA
Slow OCP	Slow over current protection (shutdown and latch after MIN/MAX timing)	280A	290A	50 ms	100 ms
Fast OCW 2	Fast over current warning (SMBAlert#)	356A	371A	5 µs	20 µs
Slow OCW 3	Slow over current warning (SMBAlert#)	260A	270A	10 ms	50 ms
OCPstby	Stby over current protection (shutdown, hiccup mode)	4.7A	6.6A	400 ms	600 ms

1. Over power protection mode shall be held for at least 100 µs before OCP shuts down the PSU.
2. Fast OCW threshold must be set below the OPP / Fast OCP threshold. Fast OCW shall hold the SMBAlert# signal asserted for 50 ms to 150 ms; then de-assert. During OCW, it will not assert any STATUS_WORD or STATUS_IOUT.
3. Slow OCW threshold must be set below the Slow OCP threshold.

Design note: The hold time for the SMBAlert# signal after an OCW1 event (fast over current warning) shall be adjustable by firmware updates in the range of 5 ms to 200 ms.

6.2. Fast Output Current Sensing for Fast OCW (Over Current Warning)

The power supply shall have a circuit to quickly assert the SMBAlert# signal when the output current exceeds the over power protection threshold in the PSU. The SMBAlert# signal must always assert before the over power protection threshold is exceeded. SMBAlert# must always latch for about 100 ms before being released. The requirements are stated in Table 6-1. Below are example circuits for implementing Fast OCW / SMBAlert#.

In Fast OCW mode, the PSU does NOT assert any of the STATUS bits so the system will take no action.

Figure 6-1 Example Low Cost Fast SMBAlert Circuit

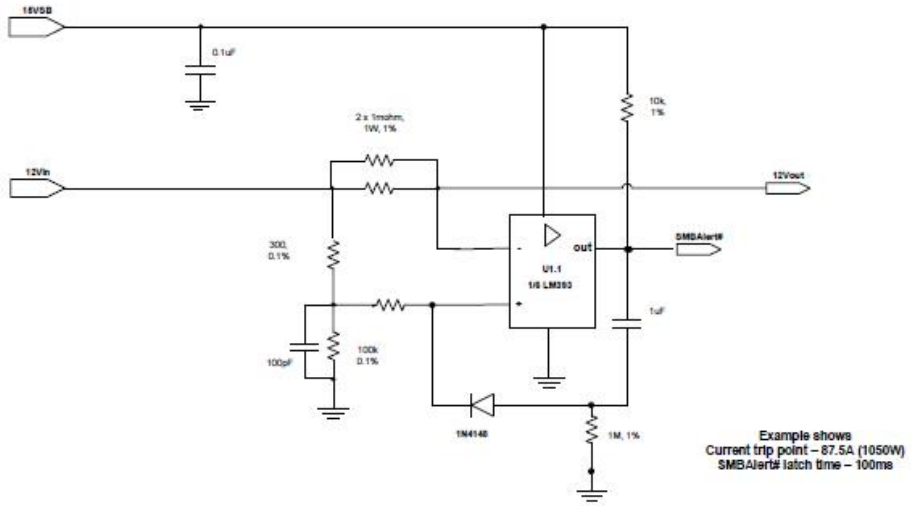
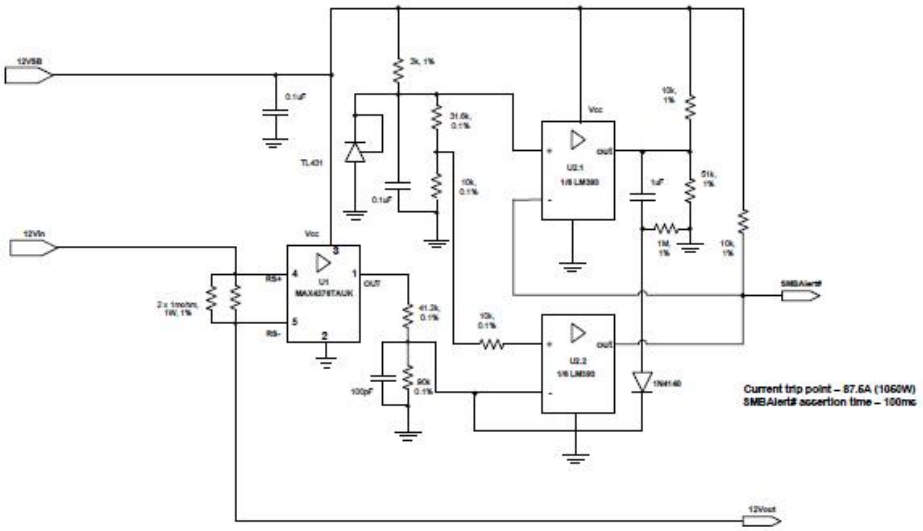


Figure 6-2 Example High Accuracy Fast SMBAlert Circuit



6.3. Over Power Protection (OPP)

The power supply shall support Over Power Protection (OPP) level low enough to protect the power supply running in this mode for repeated 100 µs durations at a 1% duty cycle. The power supply shall be stable operating at any load point from rated power up to the OPP point.

6.4. Over Voltage Protection (OVP)

The power supply over voltage protection shall be locally sensed. The power supply shall shutdown and latch off after an over voltage condition occurs. This latch shall be cleared by toggling the PSON# signal or by an AC power interruption. The values are measured at the output of the power supply's connectors. The voltage shall never exceed the maximum levels when measured at the power connectors of the power supply connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power connector. 12VSB will be auto-recovered after removing OVP limit.

Table 6-2 Over Voltage Protection (OVP) Limits

Output Voltage	MIN (V)	MAX (V)
+12V	13.5	14.5
+12VSB	13.5	14.5

6.5. Over Temperature Protection (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shut-down. OT warning SMBAlert assertion must always precede the OTP shutdown. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the 12VSB remains always on. The OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition. The OTP trip temperature level shall be at least 4 °C higher than SMBAlert over temperature warning threshold level.

6.6. PFC Over Voltage Protection (Bulk OVP)

The PFC section over voltage protection should have an independent feedback resistors and independent voltage reference from the regulation circuit. A double PFC OVP fault protection circuit is necessary.

6.7. Output Under Voltage Protection (Output UVP)

The power supply will be protected against output under voltage conditions caused by component failure, output unable to reach voltage regulation, or excessive output loading. When UVP trips; it shall de-assert DCGOOD and latch OFF the PSU.

The latch will be cleared by an AC power cycle or PSON toggle.

Table 6-3 Output Under Voltage Protection (UVP) Limits

Output Voltage	MIN (V)	NOMINAL (V)	MAX (V)	Delay Time
+12V	5.0	10.5	11.0	At least 10ms
+12VSB	5.0	10.0	10.5	At least 10ms

7. Control and Indicator Functions

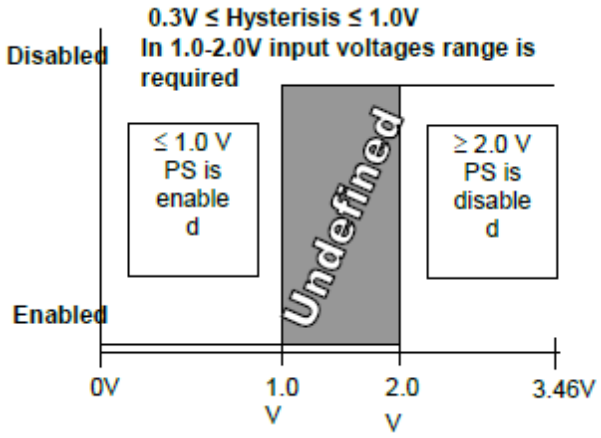
The following sections define the input and output signals from the power supply. Signals that can be defined as low true use the following convention: *Signal*# = low true

7.1. PSON# Input Signal

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the +12V p over rail. When this signal is not pulled low by the system, or left open, the outputs (except the +12VSB) turn off. This signal i s pulled to a standby voltage by a pull-up resistor internal to the power supply. Refer to Table 15 for the timing diagram

Table 7-1 PSON# Signal Characteristic

Signal Type	Accepts an open collector/drain input from the system. Pull- up to VSB located in power supply.		
PSON# = Low	ON		
PSON# = High or Open	OFF		
	MIN	**Nominal**	**MAX**
Logic level low (power supply ON)	0V	0V	1.3V
Logic level high (power supply OFF)	2.0V	3.3V	3.46V
Source current, Vpson = low			4mA
Power off delay: Tpson_off_delay			5ms
Power up delay: Tpson_on_delay	5ms		400ms
PWOK delay: T pson_pwok			5ms



7-1 PSON# Required Signal Characteristic

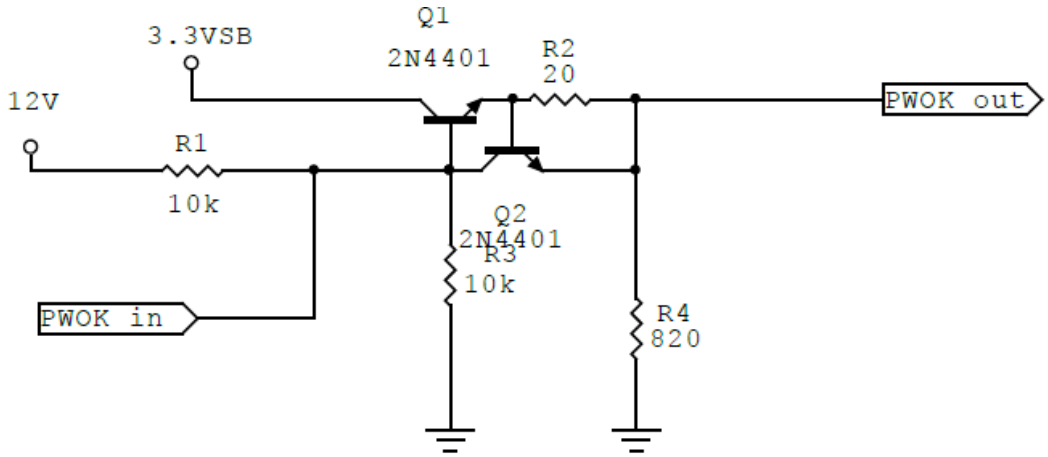
7.2. PWOK (Power OK) Output Signal

PWOK is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. See Table 7-2 for a representation of the timing characteristics of PWOK. The start of the PWOK delay time shall inhibited as long as any power supply output is in current limit.

Signal Type	**Open collector/drain output from power supply. Pull-up to VSB located in the power supply.**		
PWOK = High	Power OK		
PWOK = Low	Power Not OK		
	MIN	**Nominal**	**MAX**
Logic level low voltage, Isink=400uA	0V	0V	0.4V
Logic level high voltage, Isource=200μA	2.4V	3.3V	3.46V
Sink current, PWOK = low			400uA
Source current, PWOK = high			2mA
PWOK delay: Tpwokon	100ms		500ms
PWOK rise and fall time			100μs
Power down delay: T pwok_off	1.2ms		200ms

A recommended implementation of the Power Ok circuits is shown below.

Note: the Power Ok circuits should be compatible with 5V pull up resistor (>10k) and 3.3V pull up resistor (>6.8k)



7-2 Power OK recommended circuit

7.3. SMBAlert# Signal

This signal indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserte d due to Critical events or Warning events. The signal shall activate in the case of critical component temperature reached a warning threshold (see sec. 4.10), general failure, over-current, over-voltage, under-voltage, failed fan.

Table 7-2 SMBAlert# Signal Characteristics

Signal Type (Active Low)	**Open collector / drain output from power supply. Pull-up to VSB located in system.**		
Alert# = High	OK		
Alert# = Low	Power Alert to system		
	MIN	**Nominal**	**MAX**
Logic level low voltage, Isink=4 mA	0 V	0 V	0.4 V
Logic level high voltage, Isink=50 µA	2 V	3.3 V	3.46 V
Sink current, Alert# = low			4 mA
Sink current, Alert# = high			50 µA
Alert# rise and fall time			100 µs

7.4. Electrical Layer

The PMBus electrical driving levels shall comply with high power DC specifications given in Section 3.1.3 of SMBus Specification version 2.0.

7.5. Pull Ups

SDA and SCL pins (for I2C bus) is designed to operate at 3.3V. The main pull up resistors are provided by the system and may be connected to 3.3V only. The power supply internally has a 100K ohm pull up resistor

7.6. A0, A1

PSU Module Address line A0, A1. These signals are provided for determining the address for the specific PSU FRU and

PMbus address. The 10K ohm pull-up resistor should be located in the PSU and the pull-up voltage should be limited to 3.3V. The address line should be either float or pull low with equal to or less than 100ohm in the motherboard design.

7.7. FRU Data Format

For identification of the power supply an internal 256x8bit EEPROM with PMbus interface is used. The information in the EEPROM follows the IPMI (Platform Management FRU Information Storage Definition) guidelines Document Revision 1.1 from November 15, 1999.

8. Wakeup Redundancy, Sleep mode, and Awake Mode function

When the power subsystem is in sleep mode; only the needed power supply to support the best power delivery efficiency are ON/AWAKE. Any additional power supplies; including the redundant power supply, is in sleep state.

9. PMBus, SMBus, I2C functions

This power supply supports PMbus 1.2, and IPMI FRU functions.

10. In System Firmware Upload

The secondary side main microcontroller firmware must be able to be updated in the system using the In -System Firmware Update feature while in the ON state (i.e. with AC power present and PSON# asserted) and the update process will not cause any service interruption nor require AC cycling/PSON# toggle.
It is required for the FW images to be encrypted using AES-128 method.
The private key and firmware image management and security should follow FIPS PUB 140-3 publication and the referenced relevant NIST SP 800, ISO/IEC 24759:2017 ISO/IEC 19790:2012 and other applicable standards.

11. Environmental Requirements

11.1. Temperature

See section 2.5 for operating requirements.
Non-operating Ambient: -40°C to +70°C (Maximum rate of change of 20°C/hour)

11.2. Humidity

Operating: To 85% relative humidity (non-condensing)
Non-Operating: To 95% relative humidity (non-condensing)
NOTE: 95% relative humidity is achieved with a dry bulb temperature of 55°C and a wet bulb temperature of 54°C.

11.3. Altitude

Operating: to 5000 m
Non-operating: to 15200 m

11.4. Mechanical Shock

- The device will withstand the following imposed conditions without electrical or mechanical failure:
- Sample Size For all product types and product classes, the minimum number of samples shall be three (3) devices.
- Each tested device shall be exposed to three shocks in each of three axes. The amplitude of each shock shall be no less than 30 g with a half sine wave shape and a duration of 11 ms
- Non-operating shock:175 G ± 5% with pulse duration of 2 msec ± 10%
- Operating shock:90 G ± 5% with pulse duration of 2 msec ± 10%
- Pass Criteria: Each power and signal output of each unit under test shall be monitored continuously during the test.
- Sampling at greater than 1 millisecond periods is not permitted.
- The units under test shall operate within specification during the entire test.

11.5. Mechanical Vibration

- Operating Vibration :

Operating Vibration Profile Charts	
Frequency	**Acceleration Specification**
Hz	G2/Hz
10	0.00150
30	0.021
200	0.021
500	0.0021
	Grms = 2.4

- Non-Operating :

Non-Operating Vibration Profile Charts	
Frequency	**Acceleration Specification**
Hz	G2/Hz
5	0.052
200	0.052
500	0.003
	Grms = 3.8

- In each of 3 mutually perpendicular axes. The test duration shall be 30 minutes/axis for a total test duration of 90 minutes.
- Pass Criteria: At the conclusion of all three axes of testing, the products shall be unpackaged and visually inspected for any signs of damage. Only minor cosmetic damage that does not affect form, fit or function is allowed. Bent connector pins, damaged switches, damaged handles, labels with impaired readability, or bent or deformed sheet metal are not allowed.
- All units shall also pass a functional test.

11.6. Thermal Shock (Shipping)

Non-operating: -40°C to +70°C, 50 cycles, 30°C/min. ≥ transition time ≥ 15°C/min., duration of exposure to temperature extremes for each half cycle shall be 30 minutes.

11.7. Leakage Current & Hi-pot Testing

All units should pass the leakage current testing even when 4 power supplies are installed in system, four power modules use in redundant mode.

Any combination in one system with 8 redundant power supplies; AC leakage current is less than 3.5mA for total. The AC leakage current must be less than 0.75mA (for IEC60950), and 0x884mA peak (0.625mArms) (for IEC62368) @ 264Vac for single power supply (ES2 limits).

During DVT, PVT, all units must pass Hi-pot test: AC & DC voltage for

1. AC 3000V : primary to secondary, AC 1800V : primary to FG; (10mA, 1 minute)
2. DC 4242V: primary to secondary, DC 2500V: primary to FG. (10mA, 1 minute) Note: PCB layout must take meeting CCC 5000m into account.

12. Regulatory Agency Requirements

The power supply must comply with all regulatory requirements for its intended geographical market as computer server of Information Technology Equipment.

The power supply must meet all regulatory requirements for the intended market at the time of manufacturing. This power supply shall have below certificates for ITE category:

1. cULus
2. UL/CB+LVD COC
3. CCC 5000m
4. CB
5. CISPR Class A
6. FCC Class A
7. CE criteria B for power supply itself
8. RoHS 2.0 (Full ROHS lead free 6/6)
9. REACH 181
10. Efficiency 80plus Titanium Single Output
11. Immunity to meet ITE machine category on EN61000-4-X
12. BSMI
13. IEC 61000-4-2/4-3/4-4/4-5/4-6/4-8/4-11
14. Regulatory requirement:

Meet:

UL 62368-1

IEC 60950-1:2005 (Second Edition) + Am 1:2009 + Am 2:2013

IEC 61000-4-2:2008,IEC61000-4-3:2006/A1:2007/A2:2010,IEC 61000-4-4:2004/A1:2012

IEC 62368-1

IEC61000-4-5:2014,IEC61000-4-6:2013,IEC61000-4-8:2009,IEC61000-4-11:2004

EN55032:2012

EN55024:2010

EN 61000-3-2-:+A1: 2014

IEC 61000-4-2: 2008 Edition 2.0

EN 62368-1

EN 61000-3-3:2013

EN 61000-3-2:2014

GB4943.1-2011

GB/T9254-2008

GB17625.1-2012

CNS 14336-1(99)

CNS 13438 (95;甲) CNS15663

LVD 2014/35/EU EMC 2014/30/EU

RoHS 2011/65/EU ;2015/863/EC IEC 61984

IS 13252(Part 1)/IEC 60950-1 (BIS)

K60950-1 (KC)

KN32/KN35/KN 61000-4-3/4-4/4-5/4-6/4-11

EN55035

ICES-003 issue 7

The power supply itself meets class A with 0 or 3 dB margin of EMI limits for CE, FCC, CISPR tested with min. to full output resistance loading, and certificated with CE compliance.

The power supply, when installed in the system, shall meet immunity requirements specified in EN55024. Specific tests are to be EN61000-4-2, -3, -4, -5, -6, -8, and -11. The power supply must maintain normal performance within specified limits. Conformance must be designated with the European Union CE Marking.

Note: The UUT must be warmed above 30 minutes with max load before run Conducted & Radiated Emission test in lab. The UUT must be verified with 20%, 50%, and 100% of max load (resistor) for main DC-DC output voltage & Vsb respectively when run Conducted & Radiated Emission, Harmonic, EMI and EMS test in lab.

13. HALT Test Requirements

This power supply shall perform a HALT test in DVT stage for reliability verification.

The DUT (Device under Test) shall complete the HALT test according to the IPC-9592B appendix D standard. The sample size shall be more than 2 units for each of the test searching for the high and low operating limits, high and low destruct

limits, random vibration operating and destruct limits, voltage operating and destruct limits, current operating and destruct limits, and combining stresses cycling test. The total sample size should be more than 12 units. See the table below for sample allocation:

	HOL	HDL	LOL	LDL
Temperature	2 units		2 units	
	UOL	UDL		
Vibration	2 units			
	LOIVL	UOIVL	IVDL	
Voltage Input	2 units			
	UOOCL	OCDL		
Current Input	2 units			

Combined Stresses	2 units

The supplier shall identify and improve beyond the limits, and extend the margin until reaching the fundamental technical limit, and records the results onto the HALT report. The DUT samples shall be continuously upgraded / modified as long as the DUT can successfully improve and extend the margin before combined stresses test.

14. MTBF and Quality Data

The power supply shall have a minimum of (MTBF 400,000hours), 100% load duty cycle at 30 °C ambient, 45% RH ± 10%, 100% total output load, 200-240Vac input voltage, sea level operation per Telcordia Technologies Issue 3 or later, SR-332

14.1. Design for Reliability

All electrolytic capacitors shall be rated at 105 degrees C and have adequate rated life to meet a minimum 5 year life product requirement when operating at an ambient inlet temperature of 40 degrees C. Cooling fans shall have failure monitoring to warn of incorrect operation and predictive failure mechanism. All components de-rating and design should follow and meet IPC9592B Class II stress factor and with at least 5 years of life and endurance.

15. Fan Vibration.

Fan vibration should be well controlled to avoid large vibration. Accelerate velocity can't over 1.0 m/s_2 on any place on the surface of power supply case with the 40 degree C Ambient temperature and 100% loading with AC 115V input.

Excluding internal fan (fan is turned off), the power supply acoustic sound power should be less than 15dBA as operating on S tandby mode with no load/1A/2A, 180V to 264V input. Besides, no audible noise generates by magnetic parts, Relay, X-cap (such as MPP cap) or other parts during AC Power on/off and normal operation.

16. Serial number:

CDR-2721-2M1: 272121YWWRMSSSS