Compuware Technology Inc.

Power Supply Specification

Model: CPR-4021-2H3

Revision Histories:

Rev.	Description	Issued Date	Released by
1.0	Product Preliminary Specification	August 28, 2026	Curry Weng
1.1			
1.2			
1.3			
1.4			
1.5			
1.6			
1.7			

Specification is subject to change without notice

Approved by :　　***Checked by*** :　　***Prepared by*** :

04-0102-05B

1. Purpose

CPR-4021-2H3 PDB is compatible with both 12V output M-CRPS and CRPS with dimension of 185mm Length, 73.5mm width, 40mm Height and with maximum output power of 4000W (2+0) or 3200W (1+1).

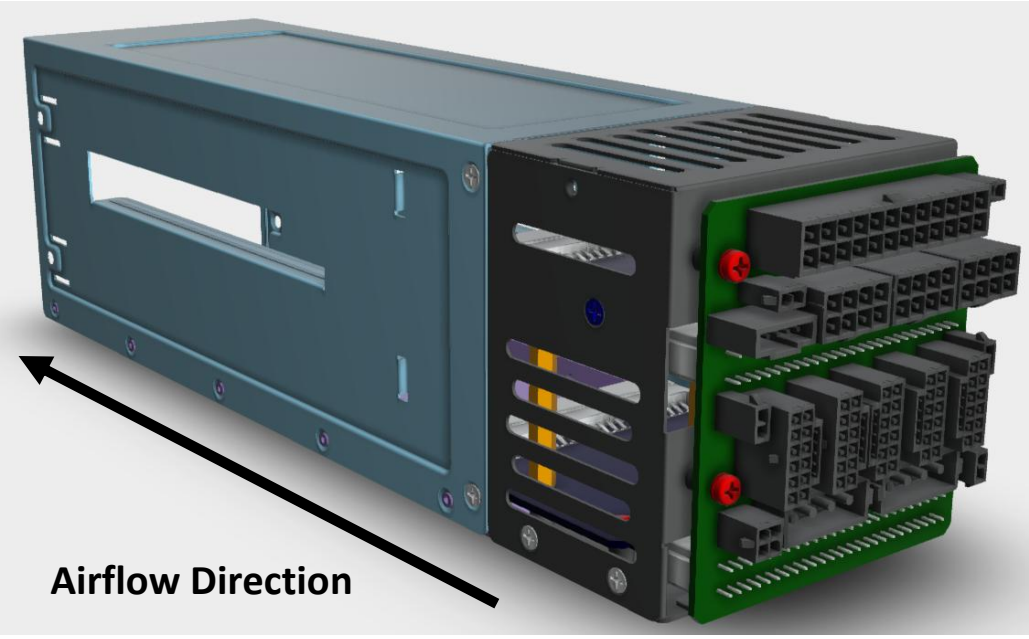
1.1 Input compatibility with CRPS and M-CRPS

PDB inputs are only compatible to CRPS or MCRPS (185m) with 12V and 12Vsb output

Recommended PSU Airflow: (AFO) Airflow Out

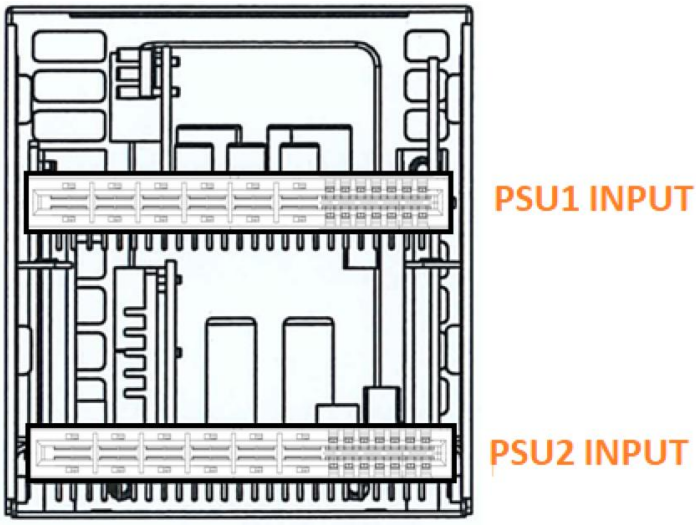
CRPS – Common Redundant Power supply

M-CRPS – Modular Hardware System- Common Redundant Power supply



Note: This PDB has no internal Fan

2.0 Input requirement



Input Pin Assignment

TOP SIDE			BOTTOM SIDE		
Name	High power connector[1]	Regular connector	Regular connector	High power connector[1]	Name
GND	P1	A1	B1	P7	GND
GND		A2	B2		GND
GND		A3	B3		GND
GND	P2	A4	B4	P8	GND
GND		A5	B5		GND
GND		A6	B6		GND
GND	P3	A7	B7	P9	GND
GND		A8	B8		GND
GND		A9	B9		GND
+12V	P4	A10	B10	P10	+12V
+12V		A11	B11		+12V
+12V		A12	B12		+12V
+12V	P5	A13	B13	P11	+12V
+12V		A14	B14		+12V
+12V		A15	B15		+12V
+12V	P6	A16	B16	P12	+12V
+12V		A17	B17		+12V
+12V		A18	B18		+12V
PMBus SDA	S1	A19	B19	S8	A0 (SMBus address)
PMBus SCL	S2	A20	B20	S9	A1 (SMBus address)
PSON#	S3	A21	B21	S10	+12Vstby
SMBAlert#	S4	A22	B22	S11	Cold Redundancy Bus
Return sense/PSKILL	S5	A23	B23	S12	12V load share bus
+12V Remote sense	S6	A24	B24	S13	-
PWOK	S7	A25	B25	S14	VINOK[2]

Notes:

1. This PDB uses high power connector.
2. Signal from installed M-CRPS unit, Not applicable for CPRS unit

3.1 Output Voltage Requirements

All outputs must maintain their regulation within the limits when measured at the output connector point in any load condition

	Output Voltage	
Output	Nominal	Regulation
+12V	12V	11.4 to 12.6V
+12Vsb	12V	11.4 to 12.6V
+5V	5V	4.75 to 5.25V
+5Vsb	5V	4.75 to 5.25V
+3V3	3.3V	3.10 to 3.49V
-12V	-12V	-11.4 to -12.6V

3.2 Output Current Requirements

All outputs must maintain their regulation as per **section 3.1** when loaded to the following loading combination:

	Output Current (2+0)	
Output	**Minimum**	**Maximum**
+12V	0.5A	333A[1,2]
+12Vsb	0.5A	Note[3]
+5V	0.3A	30A
+5Vsb	0.3A	5A
+3V3	0.3A	30A
-12V	0A	0.6A

Notes:

1. Total output power shall not exceed 4000W (Mounted 2 x 2000W PSU, 2 + 0)
2. Total output power shall also depends on the installed lower-wattage PSU(s).
3. 12vsb output current limit will depend on the installed PSU.

	Output Current (1+1)	
Output	**Minimum**	**Maximum**
+12V	0.5A	266.6A[1,2]
+12Vsb	0.5A	Note[3]
+5V	0.3A	30A
+5Vsb	0.3A	5A
+3V3	0.3A	30A
-12V	0A	0.6A

Notes:

1. Total output power shall not exceed 3200W (1+1)
2. Total output power shall also depends on the installed lower-wattage PSU(s).
3. 12vsb output current limit will depend on the installed PSU.

3.3 Output Ripple and Noise

Measurements will be made with an oscilloscope set to 20MHz bandwidth limit. Measurement is done by using 10uF Tantalum in parallel with a 0.1uf ceramic capacitor, measured directly at the output connector side (Note: care must be taken when doing measurements such as using the smallest grounding wire.

Output Ripple	
Output	**Maximum**
+12V[1]	Usually 120mV
+12Vsb[2]	Usually 120mV
+5V	50mV
+3V3	50mV
+5Vsb	50mV
-12V	-120mV

Notes:

1. 12V ripple limit are dependent on the installed PSU.
2. 12Vsb ripple limit are dependent on the installed PSU.

3.4 Output Dynamic Loading

The output voltages shall remain within the limits specified in 3.1 for the step loading and within the limits specified in 3.4 for the capacitive loading. The load transient repetition rate shall be tested between 50 Hz and 5 kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load to the MAX load shown in 3.2

Transient Load Requirements

Output	Δ Step Load Size	Load Slew Rate	Capacitive Load
+3.3 V	30% of max load	0.5 A/μs	1000 μF
+5 V	30% of max load	0.5 A/μs	1000 μF

3.5 Capacitive Loading

The power supply shall be stable and meet all requirements, except dynamic loading requirements, with the following capacitive loading ranges.

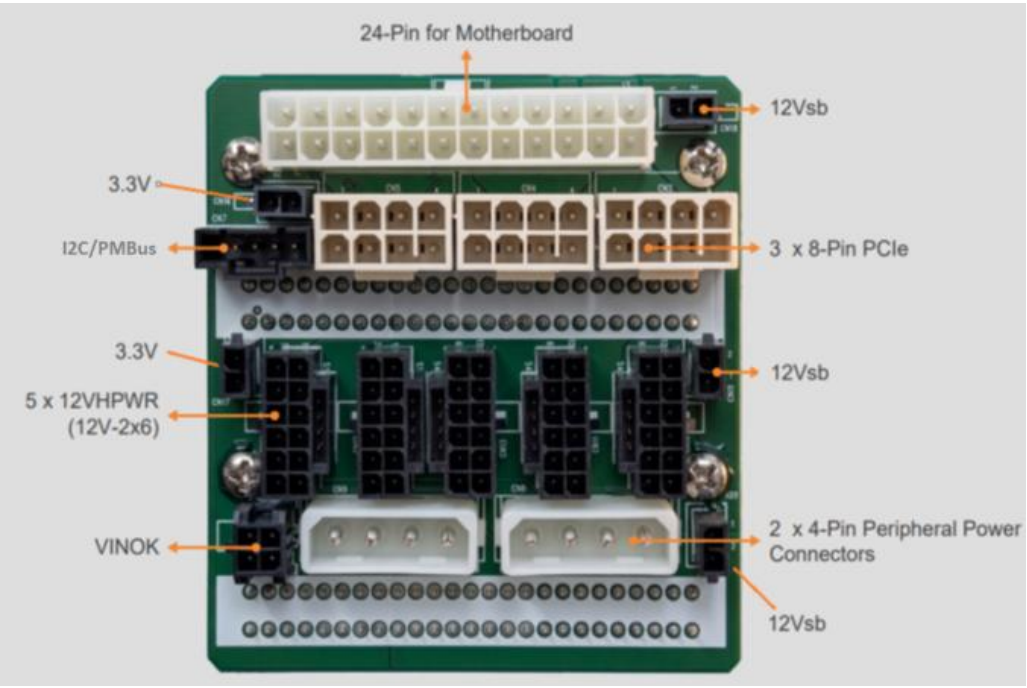
Capacitive Loading Conditions

Output	MIN	MAX	Units
+3.3 V	10	12,000	μF
+5 V	10	12,000	μF
-12 V	1	350	μF

The power distributor board shall be designed for active current sharing. Two or more than two power supplies will be paralleled in a system. Each power distributor board must be able to share

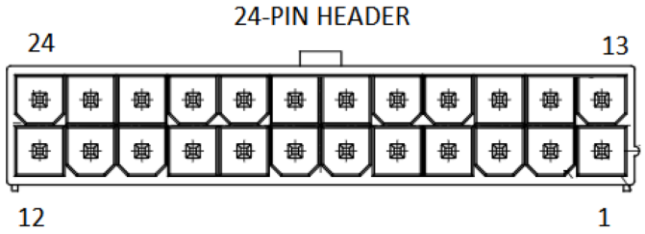
4 Output Header

Multi-Connector PCB output headers



MB 24-Pin Signal Assignment header

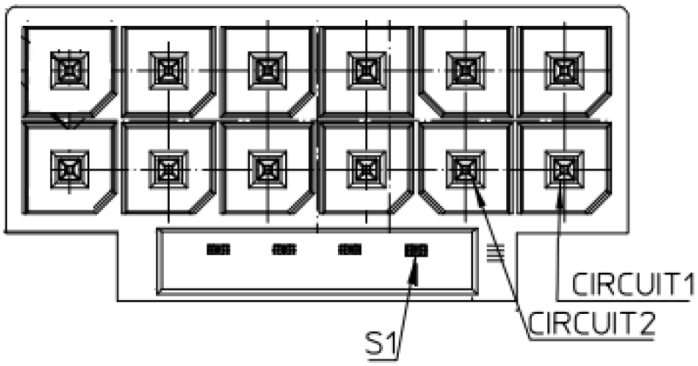
Pin	Signal	Pin	Signal
1	+3.3 V	13	+3.3 V
2	+3.3 V	14	-12 V
3	COM	15	COM
4	+5 V	16	PS_ON
5	COM	17	COM
6	+5 V	18	COM
7	COM	19	COM
8	PWR OK	20	Reserved (-5 V in ATX)
9	5 VSB	21	+5V
10	+12 V	22	+5V
11	+12 V	23	+5V
12	3.3 V	24	COM



16-pin 12VHPWR (12V-2x6) header

Pin	Signal	Pin	Signal
1	+12V	7	GND
2	+12V	8	GND
3	+12V	9	GND
4	+12V	10	GND
5	+12V	11	GND
6	+12V	12	GND
S1	N.C.	S3	GND
S2	N.C.	S4	GND

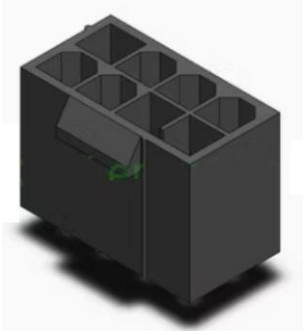
S3 and S4 set to Max power: 600W

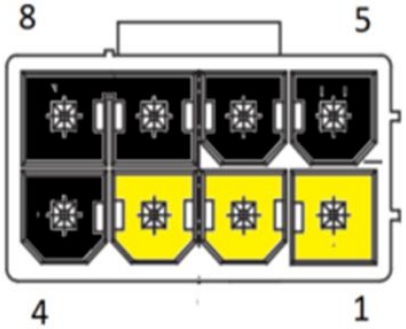


PCIE 8-Pin header

Pin	Signal	Pin	Signal
1	+12 V	5	GND
2	+12 V	6	GND
3	+12 V	7	GND
4	GND	8	GND

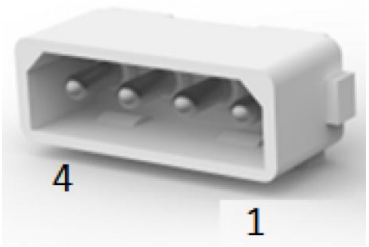
Max power: 150W





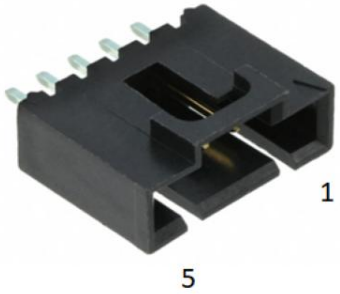
4-Pin Peripheral Power header

Pin	Signal
1	+12 V
2	GND
3	GND
4	+5 VDC



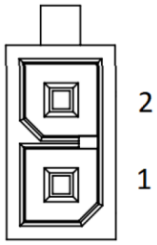
5-pin Server Signal header

Pin	Signal
1	SMBus Clock
2	SMBus Data
3	Reserved for PF
4	GND
5	Empty



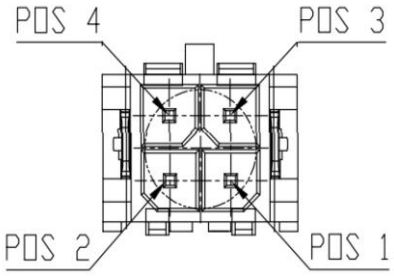
2-Pin Power header

Pin	Signal
1	+12Vsb
2	GND



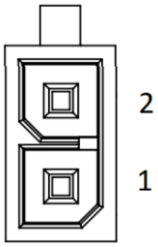
4-Pin header

Pin	Signal
1	N.C.
2	VinOK
3	GND
4	GND



2-Pin Power header

Pin	Signal
1	+3.3V
2	GND



5 Controls and Signal

These are the timing requirements for the power supply operation. The +3.3V, +5V and -12V output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 1.5 to 7ms tested with power supply. All outputs must rise monotonically.

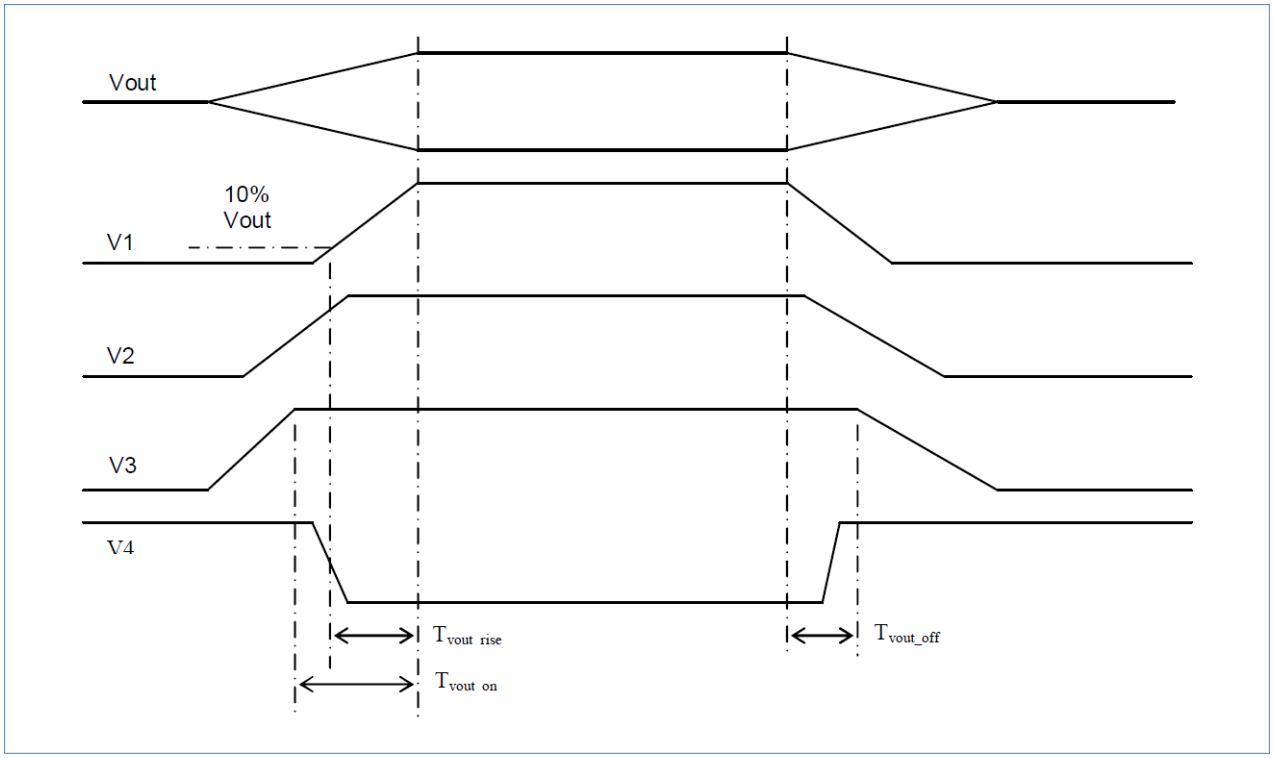
The +5 V output needs to be greater than the +3.3 V output during any point of the voltage rise. The +5 V output must never be greater than the +3.3V output by more than 2.25 V.

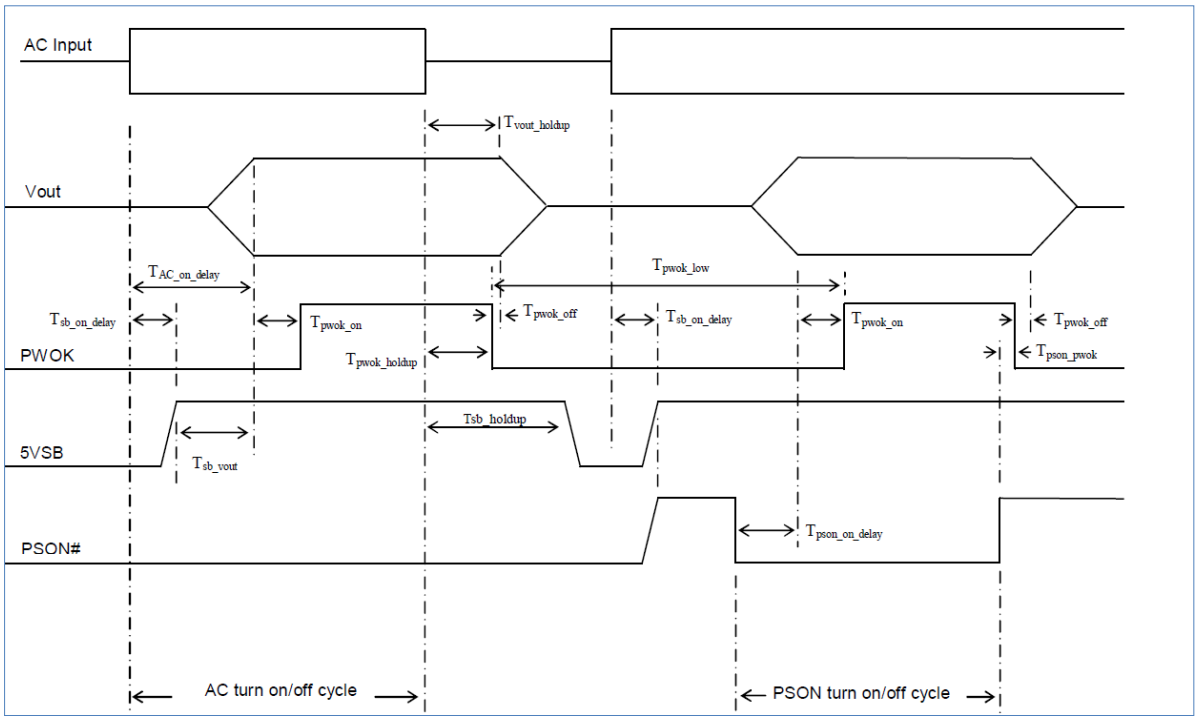
All output including the +12V main output must be in regulation within 20 ms time (Tvout_on).

Item	Description	MIN	MAX	Units
T_{vout_rise}	Output voltage 3.3V, 5V and -12V rise time from each main output.	1.5	7	ms
T_{vout_on}	All main outputs included 12V must be within		20	ms

	regulation of each other within this time.			
T vout_off	All main outputs must leave regulation within this time.		300	ms

Output Voltage Timing





Item	Description	MIN	MAX	Units
Tsb_on_delay	Delay from AC being applied to 5 VSB being within regulation.		1500	ms
T ac_on_delay	Delay from AC being applied to all output voltages being within regulation.		3000	ms

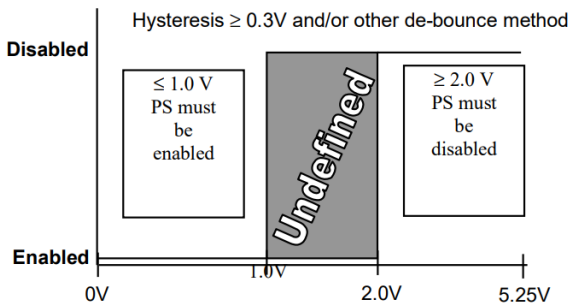
Tvout_holdup	Time all output voltages stay within regulation after loss of AC at 70% of max load	11		ms
Tpwok_holdup	Delay from loss of AC to deassertion of PWOK at 70% of max load	10		ms
Tpson_on_delay	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
T pson_pwok	Delay from PSON# deactive to PWOK being deasserted.		50	ms
Tpwok_on	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500 Depending o n the power supply	ms
T pwok_off	Delay from PWOK deasserted to output voltages (3.3 V, 5 V, 12 V, -12 V) dropping out of regulation limits. At 70% load.	1 or 0.7 depending power supply		ms
Tpwok_low	Duration of PWOK being in the deasserted state during an off/on cycle using AC or the PSON# signal.	100		ms
Tsb_vout	Delay from 5 VSB being in regulation to O/Ps being in regulation at AC turn on.	50	1000	ms
T_{sb_holdup}	Time 5VSB output voltage stays within regulation after loss of AC. At 70% load.	70		ms

4.1 PS_ON

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the +12V power rail. When this signal is not pulled low by the system, or left open, the outputs (except the +12VSB) turn off. This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply. Refer to the timing diagram

PSON# Signal Characteristic

Signal Type	**Accepts an open collector/drain input from the system. Pull- up to VSB located in power supply.**		
PSON# = Low	ON		
PSON# = High or Open	OFF		
	MIN	**Nominal**	**MAX**
Logic level low (power supply ON)	0V	0V	1.0V
Logic level high (power supply OFF)	2.0V	3.3V	3.46V
Source current, Vpson = low			4mA
Power off delay: Tpson_off_delay			5ms
Power up delay: Tpson_on_delay	5ms		400ms
PWOK delay: T pson_pwok			5ms



Logic level definition

4.2 PWOK (Power OK)

PWOK is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. See below table *for* a representation of the timing characteristics of PWOK. The start of the PWOK delay time shall inhibited as long as any power supply output is in current limit.

Signal Type	**Open collector/drain output from power supply. Pull-up to VSB located in the power supply.**		
PWOK = High	Power OK		
PWOK = Low	Power Not OK		
	MIN	**Nominal**	**MAX**
Logic level low voltage, Isink=400uA	0V	0V	0.4V
Logic level high voltage, Isource=200μA	2.4V	3.3V	3.46V
Sink current, PWOK = low			400uA
Source current, PWOK = high			2mA
PWOK delay: Tpwokon	100ms		500ms
PWOK rise and fall time			100μs
Power down delay: T pwok_off	1.2ms		200ms

5. Protection

5.1 Over Current Protection

The PDB shall have current limit to prevent +12V outputs from exceeding the values shown in Table 3. If the current limits are exceeded, the power supply shall shutdown and latch off in timing as long as good (about 200ms) with no damage occur to PDB self and power supply. The latch will be cleared by toggling the PSON# signal or by an AC power interruption. The power supply shall not be damaged from repeated power cycling in this condition. All outputs shall be protected so that no damage occurs to the power supply under a shorted output condition.

Over Current Protection

Voltage	Over Current Limit (Iout limit)
+12V	based on the installed PSU
+12Vsb	based on the installed PSU
+3.3 V	110% target; 110% minimum; 130% maximum
+5 V	120% target; 120% minimum; 135% maximum

5.2 Over Voltage Protection

The over voltage protection shall be locally sensed. The PDB shall shutdown and latch off after an over voltage condition occurs. This latch shall be cleared by toggling the PSON# signal or by an AC power interruption. The values are measured at the output of the PDB's connectors. The voltage shall never exceed

the maximum levels when measured at the power pins of the PDB output connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power pins of the power supply connector.

Over Voltage Limits

Output	MIN (V)	MAX (V)
+12V	Based on the installed PSU	
+12Vsb		
+3.3V	3.9	4.5
+5V	5.7	6.5
+5Vsb	5.7	6.5

6 Dimension

The physical size of the PDB enclosure is

L: 292.5±40, W: 78 ±0.3, H: 84 ±0.3mm **(for reference only)**

Note: Refer to mechanical outline drawing for accurate details

7 Environmental Requirements

7.1 Temperature

7.1.1 Normal Operating Ambient (at sea level):

10°C minimum (operating and in standby)

50°C maximum (operating – power supply on)

40°C maximum (standby – AC power only, power supply off) maximum rate of change is 30 degrees Celsius/hour

7.2 HUMIDITY

Operating: 20% to 90% RH

Storage: 5% to 95% RH

7.3 ALTITUDE

Operating: to 10,000 feet

Non-operating: to 35,000 feet

7.4 MTBF and Quality Data

The life requirement shall be met the following condition. And the environmental temperature is assumed to be 25°C.Normal operation (at the rated input/output): 350,000h.

8. Grounding

The ground of the pins of the power supply wire harness provides the power return path. The wire harness ground pins shall be connected to safety ground (power supply enclosure).

9. I2C addresses

The left slot of the PDB should set the lower two bits of the power supply I2C address to 00. The right slot of the PDB should set the lower two bits of the power supply I2C address to 01.

	Signal# A1 (Pin# S10)	Signal# A0 (Pin# S15)
Bottom input	Pull to GND	Pull to GND
Top input	Pull to GND	Pull to 5V

I2C address is Bottom input “00”; (A0 0V low; A1 0V low)

I2C address is Top input “01”; (A0 5V high; A1 0V low)

10. Regulatory Agency Requirements

The PDB must comply with all regulatory requirements for its intended geographical market as computer server of Information Technology Equipment.

The PDB test with power supply must meet all regulatory requirements for the intended market at the time of manufacturing. Typically this includes:

- UL, cUL
- TUV
- CE
- CCC
- FCC
- RoHS with 6/6 RoHS.

11. Serial number:

CPR-4021-2H3: 402123YWWRMSSSS