Compuware Technology Inc.

Power Supply Specification

Model: CPS-5011-4A41 (PMBus)

Revision History:

Rev.	Description	Issued Date	Released by
1.0	Release	08/14/2018	Enya Tsai
1.1	EN210818 Update Outline drawing.	09/07/2021	Enya Tsai

Specification is subject to change without prior notice

Approved by: ***Checked by:*** Steven 9/7 ***Prepared by:*** 9/7

9/7

Table of Contents

1. Purpose

This specification defines the performances of a single-phase (3-wire) power supply with wide range input AC capability (90-264VAC/47-63Hz). The parameters of this supply are defined in this specification for ITE commercial using. This specification defines max continuous output at 500W (90-264Vac input) power supply with five outputs; +3.3V, +5V, +12V1, 12V2 and +5VSB. An IEC connector is provided on the external face for AC input to the power supply. The power supply contains fans for cooling, while meeting acoustic requirements. The power supply shall have an EEPROM for storing powers supply FRU information, and meet PMBus Revision 1.2 requirement.

2. AC Input Requirements

The power supply shall incorporate universal power input with active power factor correction, which shall reduce line harmonics in accordance with the EN61000-3-2 for office business computer systems.

2.1 AC Inlet Connector

The AC input receptacle must be approved by Product Safety Regulatory Agencies and must be rated properly for the current, voltage and temperature rating. The AC input connector shall meet following requirements: IEC 320 C14 with 15A/250Vac rate.

2.2 AC Input Voltage Specifications

The power supply must operate within all specified limits over the following input voltage range. Harmonic distortion of up to 10% THD must not cause the power supply to go out of the specified limits. The power supply shall operate properly at 87 VAC input voltage to guarantee proper design margins.

Table 1: AC Input Voltage Rating

Parameter	MIN	Rated	MAX
Voltage	90 Vrms	100 – 240 Vrms	264 Vrms
Frequency	47 Hz	50 / 60 Hz	63 Hz

2.3 Input Under Voltage

The power supply shall contain protection circuitry such that application of an input voltage below the minimum specified in section 2.2 shall not cause damage to the power supply. Input voltage range for AC minimum startup voltage, 75 to 85VAC, and maximum turn off voltage range 70 to 80VAC.

2.4 Efficiency

This power supply shall meet 80PLUS Platinum efficiency requirement for 115Vac Internal multiple output. The efficiency and power factor should meet or exceed the below requirement.

Efficiency, Power Factor and THD requirement

Load (%)	115Vac		
	THD (%)	Power Factor	Efficiency (%)
20	Less than 10%	N/A	At least 90
50	Less than 5%	0.95	At least 92
100	Less than 5%	0.98	At least 89

Note : Efficiency tolerance ±0.2%

2.5 AC Line Fuse

The power supply shall incorporate one input fuse on the LINE side for input over current protection to prevent damage to the power supply and meet product safety requirements. Fuses should be fast type or equivalent to prevent nuisance trips. AC inrush current shall not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply shall not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions. The Fuse can't blow under short-circuit test.

2.6 AC Inrush

When input power is applied to the power supply any initial current surge or spike of 10ms or less will not exceed 30A peak. Any additional inrush current surges or spikes in the form of AC cycles or multiple AC cycles greater than 10ms, and less than 150ms, must not exceed 15A peak. After 150ms the AC input current must meet the input AC current requirements 2.2.

For any conditions during turn-on the inrush current will not open the primary input fuse or damage any other components.

2.7 AC Line Transient Specification

AC line transient conditions shall be defined as "sag" and "surge" conditions. Sag conditions (also referred to as "brownout" conditions) will be defined as the AC line voltage dropping below nominal voltage. Surge will be defined as the AC line voltage rising above nominal voltage.

The power supply shall meet the requirements under the following AC line sag and surge conditions.

Table 1: AC Line Sag Transient Performance

Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltage ranges	50/60 Hz	No loss of function or performance
0 to ½ AC cycle	100%	Nominal AC Voltage ranges	50/60 Hz	No loss of function or performance
0 to > ½ AC cycle	>10%	Nominal AC Voltage ranges	50/60 Hz	Loss of function acceptable, self-recoverable

Table 2: AC Line Surge Transient Performance

Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltages	50/60 Hz	No loss of function or performance
0 to ½ AC cycle	30%	Mid-point of nominal AC Voltages	50/60 Hz	No loss of function or performance

2.8 Electromagnetic compatibility (EMC) Requirements

The power supply shall meet the following electrical immunity requirements when connected to a cage with an

external EMI filter which meets the criteria defined in the latest active standard of ITE (server power category).

Performance Criteria

Level	Description
A	The apparatus shall continue to operate as intended. No degradation of performance.
B	The apparatus shall continue to operate as intended. No degradation of performance beyond spec limits.
C	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls.

2.8.1 AC Line Fast Transient Specification

The power supply shall meet the EN61000-4-4: 2004 directive and any additional requirements in IEC1000-4-4:2004 and the Level 3 requirements for surge-withstand capability, with the following conditions and exceptions:

These input transients must not cause any out-of-regulation conditions, such as overshoot and undershoot, nor must it cause any nuisance trips of any of the power supply protection circuits. The surge-withstand test must not produce damage to the power supply.

The supply must meet surge-withstand test conditions under maximum and minimum output load conditions. Meet criterion B.

2.8.2 AC Line Surge Specifications

The power supply shall meet the EN61000-4-5 directive and any additional requirements in IEC1000-4-5:2006 and the Level 3 requirements for surge-withstand capability, with the following conditions and exceptions:

These input transients must not cause any out-of-regulation conditions, such as overshoot and undershoot, nor must it cause any nuisance trips of any of the power supply protection circuits.

The surge-withstand test must not produce damage to the power supply.

The supply must meet surge-withstand test conditions under maximum and minimum output load conditions. Meet criterion A.

2.8.3 Conducted Immunity

The power supply shall comply with the limits defined in EN61000-4-6:2009 using the IEC 61000-4-6-2008 test standard and performance criteria B.

2.8.4 Radiated Immunity

The power supply shall comply with the limits defined in EN61000-4-3:2006+A1:2008+A2:2010 using the IEC 61000-4-3:2006+A1:2007+A2:2010 test standard and performance criteria B.

2.8.5 Electrostatic Discharge Susceptibility

The power supply shall comply with the limits defined in EN61000-4-2:2009 Level 3; using the IEC 61000-4-2: Edition 1.2:2001-04: 2009 level 3 test standard and performance criteria B.

The UUT must meet test condition: +/-8KV contact and +/-15KV air (for exterior and enclosure), +/-4KV contact and +/-8KV air (for signal and power pins)

2.9 AC Line Isolation Requirements

The Power supply must meet all safety agency requirements for dielectric strength.

The isolation between primary and secondary must use a) isolation transformers or b) photo-couplers or c) digital isolators or mixed a), b) and c) together and must comply with the 3000Vac (4242Vdc) dielectric strength criteria. In addition, the insulation between primary and secondary circuits, and primary to ground circuits must comply with reinforce insulation per safety standard IEC-950. Separation between the primary and secondary circuits, and primary to ground circuits, must comply with the IEC 950 spacing requirements.

The insulation impedance between AC L (or N) and FG (or chassis ground) must be greater than 1000 Mega-ohms

(1000X10^6 ohms) measured with high-resistance ohm meter.

3. DC Output Specification

3.1 Grounding

The ground of the pins of the power supply wire harness provides the power return path. The wire harness ground pins shall be connected to safety ground (power supply enclosure).

3.2 Remote Sense

The power supply may have remote sense return (Return_S) to regulate out ground drops for all output voltages; +3.3V, +5V, +12V1, 12V2 and +5VSB. The power supply may use remote sense (3.3VS) to regulate out drops in the system for the +3.3V output. The +5V, +12V1, 12V2 and +5VSB outputs only use remote sense referenced to the Return_S signal. The remote sense input impedance to the power supply must be greater than 200 Ω on 3.3VS and Return_S. This is the value of the resistor connecting the remote sense to the output voltage internal to the power supply. Remote sense must be able to regulate out a minimum of 200mV drop on the +3.3V output. The remote sense return (Return_S) must be able to regulate out a minimum of 200mv drop in the power ground return. The current in any remote sense line shall be less than 5mA to prevent voltage-sensing errors. The power supply must operate within specification over the full range of voltage drops from the power supply's output connector to the remote sense points.

3.3 Output Load Condition

The following table defines the output power and current ratings. The combined output power of all output shall not exceed the rated output power. The tables show the load ranges of the two power supply power levels. Power supply should not be damaged when any output voltage has zero loading.

Table 4：500W Load Ratings			
Load Range			
Voltage	Min. Continuous	Max. Continuous	
+3.3V	0A	12A	
+5V	0A	15A	
12V1	0.25A	21A	
12V2	0.25A	21A	
+5VSB	0 A	3.0A	

Note：

1. Maximum continuous total DC output power should not exceed 500W
2. Maximum combined continuous power of 12V combine 485W; 5V and 3.3V should not exceed 80W.

Under no load or minimum load condition, the power supply must be able to power on or off successfully. Voltage regulation level should also be maintained. No load condition to any or all voltage rails should not cause any protection circuit to be triggered.

3.3.1 Standby Output

The +5VSB output shall be present when an AC input greater than the power supply turn on voltage is applied. Main cooling fan shall be normally off when 5Vsb is on during standby mode.

3.3.2 Zero Load Stability & input power Requirements

When the power supply operates in a no load (0A) condition, it needs to meet all the output regulations without any tripping of over-voltage and there is no stress over design margin of any part. When the power supply is subsequently loaded (>0.1A), it must begin to regulate and source current without fault.

3.4 Voltage Regulation

The power supply output voltages must stay within the following voltage limits when operating at steady state and dynamic loading conditions. All outputs are measured with reference to the return remote sense (Return_S) signal. The +5V, +12V1 & 12V2, and +5VSB outputs are measured at the power supply connectors referenced to Returns. The +3.3V is measured at its remote sense signals (3.3VS) located at the signal connector.

Table 5: Voltage Regulation Limits

Parameter	MIN	NOM	MAX	Units	Tolerance
+3.3V	+3.140	+3.30	+3.46	Vrms	+5 / -5%
+5V	+4.75	+5.00	+5.25	Vrms	+5 / -5%
+12V1, V2	+11.40	+12.00	+12.60	Vrms	+5 / -5%
+5VSB	+4.75	+5.00	+5.25	Vrms	+5 / -5%

There should never be any negative voltage for all outputs and signals. During standby (PSON=off), all outputs, except +5VSB, should be below 50mV.

3.5 Dynamic Loading

he output voltages shall remain within the limits specified in section 3.3 for the step loading and within the limits specified in section 3.5 for the capacitive loading. The load transient repetition rate shall be tested between 50 Hz and 5 kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load to the PEAK load shown in

Table 6: Transient Load Requirements

Output	∆ Step Load Size	Load Slew Rate	Capacitor Load
+3.3V	30% of max load	0.5A/us	10uF-12000uf
+5V	30% of max load	0.5A/us	10uF-12000uf
+12V1,+12V2	65% of max load	0.5A/us	10uF-12000uf
+5VSB	25% of max load	0.5A/us	1uF-350uf

3.6 Capacitance Loading

The power supply shall be stable and meet all requirements with the following capacitive loading ranges.

Table 7: Capacitive Loading Conditions			
Output	MIN	MAX	Units
+3.3V	10	12,000	uF
+5V	10	12,000	uF
+12V1,12V2	10	12,000	uF
+5VSB	1	350	uF

3.7 Ripple / Noise

The maximum allowed ripple / noise output of the power supply is defined in Table 8 Ripple / Noise below. This is measured over a bandwidth of 0Hz to 100MHz at the power supply output connector. A 10μF tantalum capacitor in a parallel with a 0.1μF ceramic capacitor is placed at the point of measurement.

Table 8 Ripple and Noise

	+3.3V	+5V	+12V1, V2	+5VSB	
Ripple	50mVp-p	50mVp-p	120mVp-p	50mVp-p	

3.8 Timing Requirements

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits. (Tvout_rise) within 2 to 20ms; except for 5VSB which is required to rise from 10% to regulation limits within 1 to 20ms. The +3.3V, +5V, and +12V output voltages should start to rise at about the same time. All output shall rise monotonically. The +5V output needs to be greater than the +3.3V output during any point of the voltage rise. The +5V output must never be greater than the +3.3V output by more than 2.25V. Each output voltage shall reach regulation within 20ms (Tvout_on) of each other during turn on of the power supply. Each output voltage shall fall out of regulation within 400ms (Tvout_off) of each other during turn off. Figure 1 and figure 2 show the turn ON and turn OFF timing requirements. In Figure 2 the timing is shown with both AC and PSON# controlling the ON/OFF of the power supply.

Table 9: Output Voltage Timing

ITEM	DESCRIPTION	MIN	MAX	UNITS
Tvout_rise	Output voltage rise time from each main output	2	20	ms
	Output voltage rise time for the 5VSB output.	1	20	ms
Tvout_on	All main outputs must be within regulation of each other		20	ms
Tvout_off	All main outputs must leave regulation within this time		400	ms

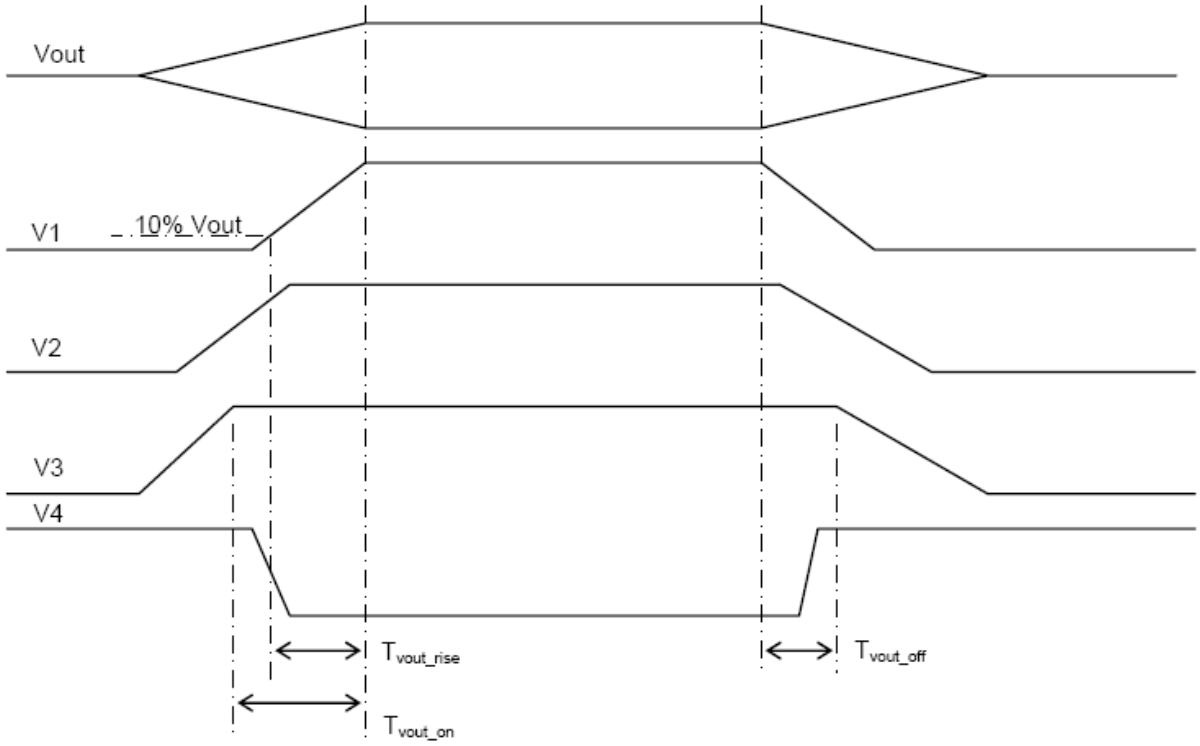


Figure 1 Output Voltage Timing

Table 10 Turn On / Off Timing

ITEM	DESCRIPTION	MIN	MAX	UNITS
T sb_on_delay	Delay from AC being applied to 5VSB being within regulation		1500	msec
T ac_on_delay	Delay from AC being applied to all output voltages being within regulation		2500	msec
T vout_holdup	Time all output voltages, including 5VSB, stay within regulation after loss of AC. Tested at 75% of maximum load and over 100-240VAC input	17		msec
T pwok_holdup	Delay from loss of AC to desertion of PWOK. Tested at 75% of maximum load and over 100-240VAC input	16		msec
Tpson_on_delay	Delay from PSON# active to output voltages within regulation limits.	5	400	msec
T pson_pwok	Delay from PSON# deactivate to PWOK being disserted.		50	msec
T pwok_on	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	msec
T pwok_off	Delay from PWOK disserted to output voltages (3.3V, 5V, 12V1 & V2, 5VSB) dropping out of regulation limits. Tested at 75% of maximum load and over 100-240VAC input	1		msec
T pwok_low	Duration of PWOK being in the disserted state during an	100		msec

	off/on cycle using AC or the PSON signal.			
T sb_vout	Delay from 5 VSB being in regulation to O/Ps being in regulation at AC turn on	50	1000	msec
Tsb_holdup	Time 5VSB output voltage stays within regulation after loss of AC	70	5000	msec

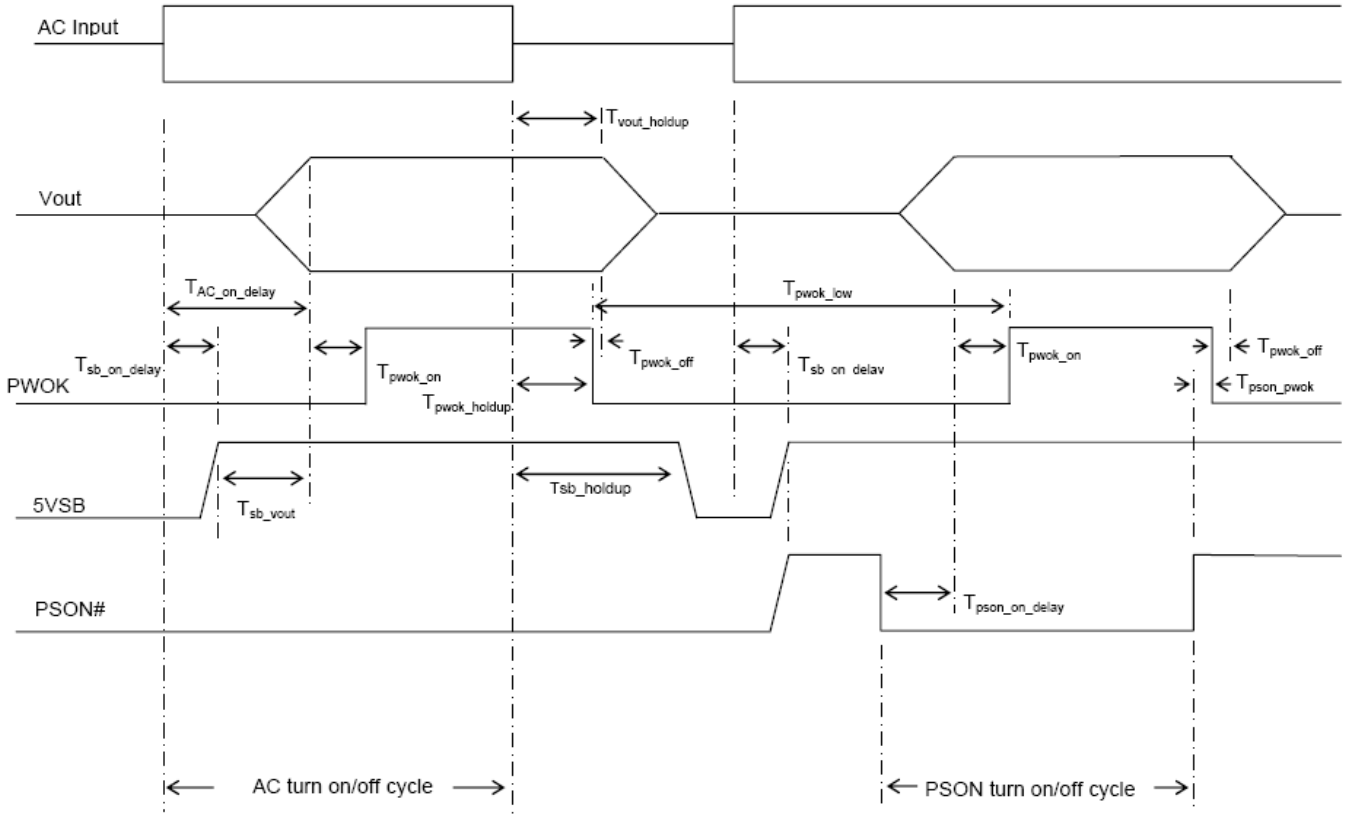


Figure 2 Turn on/off Timing

3.8.1 +5 VDC / +3.3 VDC Power Sequencing

The +12V DC and +5V V DC output levels must be equal to or greater than the +3.3V DC output at all time during power-on and normal operation. The time between any output of +12V DC and +5V DC reaching its minimum in-regulation level and +3.3V DC reaching its minimum in-regulation level must be less than or equal to 20ms.

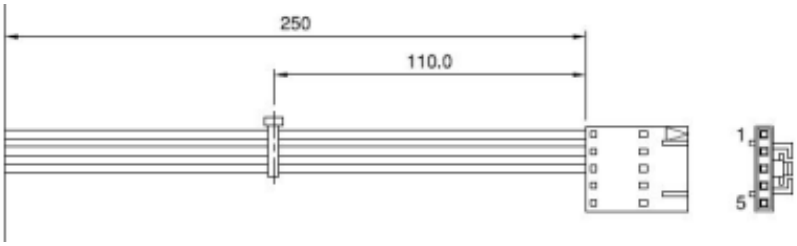
3.9 Output connector

For 24pin, 8pin, 4pin connectors, terminal contacts, they should use high current contact Molex 44476-1111 or equivalent.

For 4pin HD contacts use Tyco 61314-1 or equivalent.

3.9.1 24Pin output

The below image is just for reference.



Cable lengths tolerance +/-10mm.

24-pin: 25cm +/-1cm;

4+4 8-pin: 25cm +/-1cm

HDD right angle P5: 25cm +/-1cm;

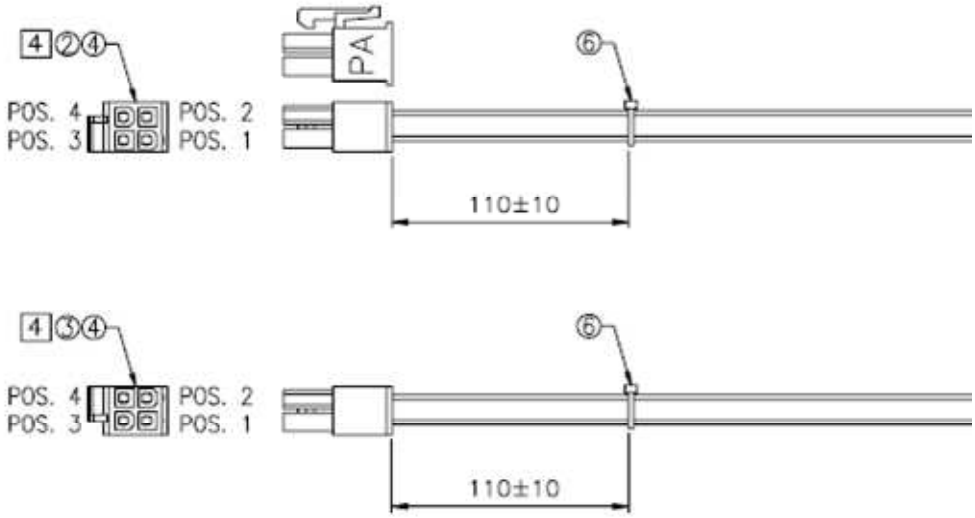
SATA right angle P6: 25cm +/-1cm;

I2C Cable: 25cm +/- 1cm

3.9.2 4+4 8Pin Connector Detail

4+4 8pin housings use Yestone: 9357-08-L and 9357-08-R or equivalent. Terminal uses 44476-1111 or equivalent.

Example drawing below:



3.9.3 Server Signal Connector (I2C/SMBus/PMBus)

For server systems with SMBus/PMBus/I2C features, the power supply may have an additional connector, which provides serial SMBus for FRU data and remote sense on 3.3V and Return.

Connector housing: 5-pin Molex 50-57-9405 or equivalent

Contacts: Molex 16-02-0088 or equivalent

Server Signal Connector

Pin	Signal	24 AWG Color
1	SMBus/PMBus Clock	White/Green Stripe
2	SMBus/PMBus Data	White/Yellow Stripe
3	SMBAlert	Red
4	No connect	No connect
5	No connect	No connect

4. Protection Circuits

Protection circuits inside the power supply shall cause only the power supply's main outputs to shutdown. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15sec and a PSON# cycle HIGH for 5sec shall be able to reset the power supply.

4.1 Over Current Limit

The power supply shall have current limit to prevent the +3.3V, +5V, 12V1/V2 and 5Vsb outputs from exceeding the values shown in Table11. If the current limits are exceeded, the power supply shall shutdown and latch off in timing (within 60-100ms) with no damage occur to PDB self and power supply. The Latch will be cleared by toggling the PSON # signal. The power supply shall not be damaged from repeated power cycling in this condition. Those outputs shall be protected so that no damage occurs to the power supply under a shorted output condition.

The +5VSB shall be protected and under over current limitation or shorted conditions so that no damage can occur to the power supply. 5VSB over current protection should be in hiccup mode (with at least 500ms off duty hiccup period) with OCP trigger delay of 60-100ms to prevent mis-triggering of protection due to surge output loading current.

Table 11 ：Over current Protection	
Voltage	Over Current Limit (I out Limit)
+3.3V	110 % minimum , 150% maximum
+5V	110 % minimum , 150% maximum
+12V1,+12V2	110 % minimum , 150 % maximum
+5Vsb	4.4A minimum , 6.5A maximum

Note: Over current protection should not be triggered during the peak current duration and within the peak current limit as stated in table 4.

4.2 Over Voltage Protection

The power supply over voltage protection shall be locally sensed. The power supply shall shutdown and latch off after an over voltage condition occurs.

This latch shall be cleared by toggling the PSON # signal. Table12 contains the over voltage limits. The values are

measured at the output of the power supply's connectors. The voltage shall never exceed the maximum levels when measured at the power pins of the power supply connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power pins of the power supply connector.

Table 12：Over Voltage Limits		
Output Voltage	**MIN (V)**	**MAX (V)**
+3.3V	3.9	4.5
+5V	5.7	6.5
+12V1,+12V2	13.3	14.5

4.3 Over Temperature Protection

The power supply will be protected against over temperature conditions cause by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shutdown. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically by PSON signal on/off status. The OTP circuit must have built in hysteresis such that the power supply will not oscillate on and off due to temperature recovering condition. The OTP trip level shall have a minimum of 4 degree C of ambient temperature hysteresis.

5. Control and Indicator Functions

The following sections define the input and output signals from the power supply. Signals are defined as low true use the following convention: signal$^{\#}$ = low true

5.1 PSON$^{\#}$

The PSON$^{\#}$ signal is required to remotely turn on/off the power supply. PSON$^{\#}$ is an active low signal that turns on the +3.3V, +5V, +12V1 and +12V2 power rails. When this signal is not pulled low by the system, or left open, the outputs (except the +5VSB) turn off. This signal is pulled to a standby voltage by a pull- up resistor internal to the power supply. Refer to Figure 2 Turn on / off Timing for timing diagram. For manufacturing quality assurance, ON/OFF cycle should be tested with an ON/OFF cycle period of 6 seconds or less, with 50% PSON duty cycle logic low, another remaining 50% PSON duty cycle logic high. However, the product should be successfully turned on/off without any timing constrains.

Table 14 PSON$^{\#}$ Signal Characteristics

Signal Type	Accepts an open collector/drain input from the system. Pull-up to VSB located in power supply.		
PSON# = Low	ON		
PSON# = Open or High	OFF		
	MIN	MAX	Nominal

Logic level low (power supply ON)	0 V	1.0 V	0 V

Logic level high (power supply OFF)	2.0 V	5.25 V	5 V
Source current, Vpson = low		4 mA	
Power up delay: Tpson_on_delay	5 ms	400 ms	
PWOK delay**:** Tpson_pwok		50 ms	

5.2 PWOK (Power OK)

PWOK is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be dearest to a LOW state. See Figure 2 On/ Off Timing for a representation of the timing characteristics of PWOK. The start of the PWOK delay time shall inhibited as long as any power supply output is in current limit.

Table 15 PWOK Signal Characteristics

Signal Type	Open collector/drain output from power supply. Pull-up to the located in power supply.		
PWOK = High	Power OK		
PWOK = Low	Power Not OK		
	MIN	MAX	Nominal
Logic level low voltage, Isink = 4mA	0V	0.4V	0V
Logic level high voltage, Isource = 200μA	2.4V	5.25V	5V
PWOK delay: T pwok_ON	100ms	500ms	
PWOK rise and fall time	*	100μsec	
Power down delay: T pwok_off	1ms	200ms	

6. MTBF

The power supply shall have a minimum MTBF at continuous operation of 1) 200,000 hours at 100% load and 50 degree C, as calculated b Bellcore RPP, or 2) 300,000 hours demonstrated at 100% load and 50 degree C.

7. Temperature Requirement

The power supply shall operate within all specified limits over T_{op} temperature range. All airflow shall pass through the power supply and not over the exterior surfaces of the power supply.

Table 17：Thermal Requirements

Item	Description	MIN	MAX	Units
T_{op}	Operating temperature range	0	50	Degree C
T_{non-op}	Non-operating temperature range	-10	70	Degree C

The power supply must meet UL enclosure requirements for temperature rise limits. All sides of the power supply, with exception to the air exhaust side, must be classified as “ Handle, Knobs, grips, etc. held for short periods of time only “.

8. Connectors and Pin Assignment

See 3.9. Output Connector

9. Compliance Requirements

The power supply must comply with all regulatory requirements for its intended geographical market as computer server of Information Technology Equipment.

The power supply must meet all regulatory requirements for the intended market at the time of manufacturing. This power supply shall have below certificates for ITE category:

1. UL
2. C-UL
3. UL/CB+LVD COC
4. CCC 5000m
5. CISPR Class B
6. FCC Part 15, subpart B, Class B
7. CE criteria B for power supply itself
8. RoHS (Full ROHS lead free 6/6)
9. Efficiency 80 Plus Platinum Multi Output 115Vac
10. Immunity to meet ITE machine category on EN61000-4-X
11. BSMI
12. REACH
13. Regulatory requirement:

Meet:

UL 62368-1 2nd Edition Am 1 and CSA C22.2 No.60950-1-07 2nd Edition

IEC 62368-1:2005 (Second Edition) + Am 1:2009 + Am 2:2013

IEC 61000-4-2:2008,IEC61000-4-3:2006/A1:2007/A2:2010,IEC 61000-4-4:2004/A1:2010

IEC61000-4-5:2005,IEC61000-4-6:2008,IEC61000-4-8:2009,IEC61000-4-11:2004

EN55022:2012 Class A

EN55024:2010

EN 61000-3-2-:2014

EN 61000-3-3:2013

GB4943.1-2011

GB9254-2008(Class A)

GB17625.1-2012

CNS 14336-1(99)

CNS 13438 (95;乙)

The power supply itself meets class B of EMI limits for CE, FCC, CISPR tested with min. to full output resistance loading, and certificated with CE compliance.

The power supply, when installed in the system, shall meet immunity requirements specified in EN55024:2010 Specific tests are to be EN61000-4-2, -3, -4, -5, -6, -8, and -11. The power supply must maintain normal performance within specified limits. Conformance must be designated with the European Union CE Marking. Specific immunity level requirements are left to customer requirements.

10. Environmental Requirements

Temperature

The power supply shall operate within all specified limits over T_{op} temperature range. All airflow shall pass through the power supply and not over the exterior surfaces of the power supply.

Table 17：Thermal Requirements

Item	Description	MIN	MAX	Units
T_{op}	Operating temperature range	0	50	Degree C
T_{non-op}	Non-operating temperature range	-10	70	Degree C

The power supply must meet UL enclosure requirements for temperature rise limits. All sides of the power supply, with exception to the air exhaust side, must be classified as “Handle, Knobs, grips, etc. held for short periods of time only.

Humidity:

Operating : 20% to 90% RH, Non-condensing

Storage : 5% to 95% RH, Non-condensing

Altitude:

Operating: to 16,500 feet (5,000 meters)

Non-operating: to 35,000 feet (10,580 meters)

11. I^2C

This power support supports both I2C function and PMBus. With different addressing, the user should able to use either Super Micro I2C FRU or PMBus commands.

I2C Signal Connector Pin Definition

Pin	Signal	24 AWG Color
1	SMBus Clock	White/Green Stripe
2	SMBus Data	White/Yellow Stripe
3	SMBAlert	Red

4	No connect	
5	No connect	

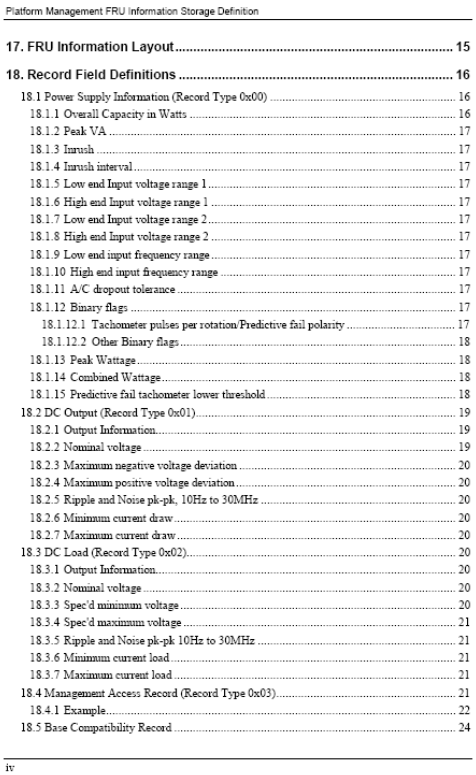
Slave address will be 0x70 (default)

For non-redundant power supply, the slave address for I2C function should be 0x70.

The power supply can be read and written to as if it's a 2k bit (256 byte) I2C EEPROM. The power supply must support: Byte write and Random read. Read and write must work at speeds up to 100 kHz. This bus shall operate at nominal voltage 3.3V but be tolerant of 5V signaling.

All the data stored in the power supply follows FRU spec, IPMI, Platform Management FRU information Storage Definition v1.0.

FRU spec attached below:



Platform Management FRU Information Storage Definition

iv

The "Chassis Info" and "Board Info" are not to be implemented. The "Common Header" and "Product Area" are required.

For the "Multiple Record" area, the power supply should implement the "Power Supply Information"(section 18.1), and multiple "DC Output" section as needed.

For the “Product Info” area must began from offset location 0x18 (offset 0x04 product information offset must contains value of 0x03).

The “Internal Use” section, defined as follows:

Offset		Result of a read
0x09	Temperature	Value to represent the current temperature of the hottest spot inside the power supply This is an unsigned integer value in Celsius.
0x0A	Fan 1 speed (main fan)	Value to represent the RPM of the power supply fan #1 This should be the fan pulse count in 262 ms. We are assuming that two fan pulses equal one rotation. The system software will convert this value, to fan RPM, using: RPM=(1/0.262) *(Fan Pulse Count * 60 /2)
0x0B	Fan 2 speed (secondary fan if available)	Value to represent the RPM of the power supply fan #1 This should be the fan pulse count in 262 ms. We are assuming that two fan pulses equal one rotation. The system software will convert this value, to fan RPM, using: RPM=(1/0.262) *(Fan Pulse Count * 60 /2) If fan 2 is not available, default value 0x00
0x0C	Power Status	Value to represent DC GOOD status byte = hex 01 means DC GOOD byte = 00 means no DC output
0x0D	Temperature High Limit (hot spot)	Value is fixed and should be the highest acceptable temperature that the power supply can sustain based on offset 09. This value is for information display purpose only and is independent from protection or fan control design. Modifying this byte will not affect the power supply operation.
0x0E	Fan 1 speed Low Limit	Value is fixed and should be the lowest fan #1 RPM acceptable. Fan 1 speed shall never be lower than this byte during PSON=on. This value is for information display purpose only and is independent from protection or fan control design. Modifying this byte will not affect the power supply operation.
0x0F	Fan 2 speed Low Limit (if secondary fan is available)	Value is fixed and should be the lowest fan #2 RPM acceptable If fan 2 is not available, default value 0x00 Fan 2 speed shall never be lower than this byte during PSON=on. This value is for information display purpose only and is independent from protection or fan control design. Modifying this byte will not affect the power supply operation.
0x10	Reserved	
0x11	Reserved	
0x12	Reserved	
0x13	Reserved	
0x14	AC RMS current	This byte, divided by 16, is the AC (RMS) input current.

0x15	DC output current (optional)	This byte is the DC output current. If this function is not available, default value is 0x00

0x16	Firmware version	Example: version 2.0 is encoded as 0x20 Anything less than 2.0 (0x20) found at this location will be reported as version 1.0 by health monitoring software Default initial value 0x10
0x17	FRU file revision	Integer only
0xF0	AC current limit	AC current upper limit; This byte, divided by 16, is the AC input current limit This value is for information display purpose only and is independent from protection or control logic design. Modifying this byte will not affect the power supply operation.
0xF1	+12V DC current limit	+12V DC current upper limit; scale factor: this byte is the DC (+12V) output current. This value is for information display purpose only and is independent from protection or control logic design. Modifying this byte will not affect the power supply operation
0xF2	Power supply output wattage rating	Power supply output wattage rating; lower byte. If the output wattage changes according to different AC input voltage range, this output should reflect accordingly.
0xF3	Power supply output wattage rating	Power supply output wattage rating; higher byte. If the output wattage changes according to different AC input voltage range, this output should reflect accordingly.
0xF4	Input voltage	Real time 100-240Vac input voltage reading (for readings above 255Vac, it should report 255Vac)
0xF5	Real time Input power (lower byte)	Real time Input power in watt (lower byte) (example 0x01F4=500W)
0xF6	Real time Input power (higher byte)	Real time Input power in watt (higher byte)
0xFA	Black box record 1	Reserved for black box record function
0xFB	Black box record 2	Reserved for black box record function
0xFC	Black box record 3	Reserved for black box record function
0xFD	Black box record 4	Reserved for black box record function
0xFE	Black box record 5	Reserved for black box record function
0xFF	Write protection Control	This byte controls whether the FRU is writeable or read only. When this byte content is 0x88, the FRU is writeable. Otherwise, only byte 0xFF can be modified. value= 0x88 is FRU writeable mode Any other value, FRU is read only except address 0xFF can be modified. Default value for this byte is read only, 0x00. After AC Lost or power on/off, this byte should not be reset and should remain to whatever the latest previous value is.

The power supply will support the “byte write” procedure defined in the I2C EEPROM spec.

Read only bytes --- writes to the following bytes should be ignored:

Offset	
0x09	Temperature

0x0A	Fan 1 speed (main fan)

0x0B	Fan 2 speed (secondary fan if available)
0x0C	Power Status
0x14	AC RMS current
0xF4	Input voltage
0xF5	Real time Input power (lower byte)
0xF6	Real time Input power (higher byte)

I2C auto-recovery feature:

In a normal I2C transaction, there will be 8 bytes of transmission plus an ACK (acknowledge) byte, for a total of 9 clock cycles. ACK is done by pulling down the SDA line. If there is a missing clock cycle, the chip doing the ACK will hold down the SDA line indefinitely and hanging the I2C bus. The power supply needs to prevent the above scenario from happening. If the I2C bus SDA or SCL is stuck low for more than 25 ms, the power supply should reset either its I2C communication module, or itself.

The power supply I2C microcontroller should not latch the system I2C bus by pulling SDA or SCL line low for more than 25 ms.

The power supply needs to have 4.7k Ohm internal pull up on the SDA or SCL lines and operate with 3.3V nominal voltage level.

12. PMBus

The PMBus specification is based on the PMBus specification parts I and II, revision 1.1 and 1.2.
PMBus Power System Management Protocol Specification Part I – General Requirements, Transport and Electrical Interface; Revision 1.2; Reference: http://PMBus.org/specs.html

PMBus Power System Management Protocol Specification Part II – Command Language; Revision 1.2; Reference: http://PMBus.org/specs.html

System Management Bus (SMBus) Specification version 2.0; Reference: http://smbus.org/specs/

12.1 Addressing

The power supply PMBus device address locations are shown below. For no-redundant systems the power supply device address location should be 78h.

System addressing	0/0			

Power supply PMBus™ device	78h			

Note: Non-redundant power supplies will use the 0/0 address location, 78h.

12.2 Hardware

The device in the power supply shall be compatible with both SMBus 2.0 'high power' specification for I^2C V_{dd} based power and drive (for Vdd = 3.3V). This bus shall operate at 3.3V but be tolerant of 5V signaling.

The power supply needs to have >4.7k Ohms internal pull up to 3.3V on the SDA or SCL lines and operate with 3.3V nominal voltage level. The equivalent impedance on the SDA or SCL lines measured from I2C bus between the I2C output connector to 3.3V must be greater than 4.7K ohms when SDA & SCL is operating.

One pin is the Serial Clock [SCL] (PSM Clock). The second pin is used for Serial Data [SDA] (PSM Data). Both pins are bi-directional, open drain signals, and are used to form a serial bus. The circuits inside the power supply shall derive their power from the standby output.

The PMBus device shall be on whenever AC power is applied to the power supply or a parallel redundant power supply in the system.

1000ns maximum rise time for SDA and SCL
300ns maximum fall time with a 400pF capacitive load for SDA and SCL
10ns minimum fall time with a 20pF capacitive load for SDA and SCL

SDA and SCL signal should have less than 300mVp-p ripples and noise. This ripple and noise is measured with 10-100MHz bandwidth and without adding any external capacitor. During the measurement, the SDA and SCL bus connection is left open and the bus is idle at nominal voltages.

12.3 Data Speed

The PMBus device in the power supply shall operate at 15Khz to 100khz and avoid using clock stretching that can slow down the bus. For example, the power supply can clock stretch while parsing a command or a power supply servicing multiple internal interrupts or NACK may require some use of clock stretching. Unsupported commands may respond with a NACK but must always set the communication error status bit in STATUS_CML.

The PMBus device shall support SMbus cumulative clock low extend time (Tlow: sext) if < 25ms. This requires the device to extend the clock time no more than 25ms between START and STOP for any given message.

12.4 Bus Errors

The PMBus device shall support SMBus clock-low timeout (Ttimeout). This capability requires the device to abort any transaction and drop off the bus if it detects the clock being held low for > 25ms, and be able to respond to new transaction 10ms later.

The device must recognize SMbus START and STOP conditions on any clock interval. (These are requirement of the SMBus specifications, but are often missed in first-time hardware designs.) The device must not hang due to 'runt clocks', 'rut data', or other out-of-spec bus timing. This defined as signals, logic-level glitches, setup or hold times that are shorter than the minimums specified by the SMBus specification. The device is not required to operate normally, but must return to normal operation once 'in spec' clock and data timing is again received. Note if the device' misses' a clock from the master due to noise or other bus errors, the device must continue to accept 'in spec' clocks and re-synch with the master on the next START or STOP condition.

12.5 Commands

The following PMBus commands shall be supported for the purpose of monitoring currents, voltages, and power. All data should use the linear data format as documented in PMBus spec.

The Linear Data Format is a two byte value with:

- An 11 bit, two's complement mantissa and
- A 5 bit, two's complement exponent (scaling factor).

The format of the two data bytes is illustrated in Figure 4.

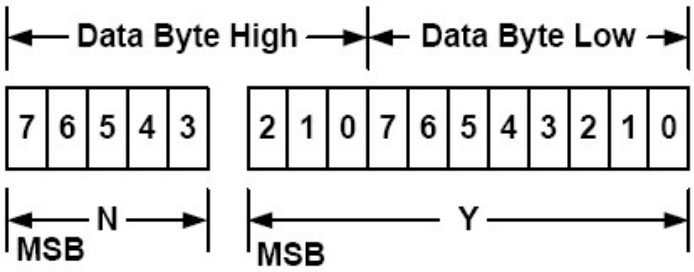


Figure 4. Linear Data Format Data Bytes

The relation between *Y*, *N* and the "real world" value is:

$X = Y \cdot 2^N$

Where, as described above:

X is the "real world" value;

Y is an 11 bit, two's complement integer; and

N is a 5 bit, two's complement integer.

Devices that use the Linear format must accept and be able to process any value of *N*.

PMBus command	Command Offset location	Byte size	Description	Query Command Response
PAGE	0x00	1	For setting the memory page for CLEAR_FAULT command. Setting a PAGE value of FFh is used to clear all status bits in all PAGEs with CLEAR_FAULT command. The default value for this byte is FFh(all pages)	0xE0
CLEAR_FAULTS	0x03	1	Writing any value into this byte will reset all the fault status at a given PAGE. If the PAGE is set to FFh; all STATUS bits in all PAGEs shall be cleared.	0xC0
PAGE_PLUS_WRITE	0x05	Variable	used with STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT	0xC0
PAGE_PLUS_READ	0x06	Variable	used with STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT, STATUS_WORD	0xA0
CAPABILITY	0x19	1	Provides a way for a host system to determine some key capabilities of a PMBus device	0xA0

QUERY	0x1A	1 with block write read	Used to determine if the power supply supports a specific command	0xA0
SMBALERT_MASK	0x1B	Variable	Used to prevent a warning or fault condition from asserting the SMBALERT# Signal. The masks can be changed by user.	0xE0
VOUT_MODE	0x20	1	determines the format of Voltage output (Linear, direct, or VID), also set the mantissa	0xA0
COEFFICIENT	0x30	5 with block write read	The system shall use this to read the values of m, b, and R used to determine READ_EIN accumulated power values.	0xE0
FAN_CONFIG_1_2	0x3A	1	Returns the configuration of Fan 1 and Fan 2 in the power supply	0xE0
FAN_COMMAND_1	0x3B	2	Allows system to request fans in the power supply to be set to the defined duty cycle. The system cannot cause the power supply fan to run slower than the power supply needs for cooling. This data should be in linear format. Example (32h=50% duty, 64h=100% Duty).	0xE0
FAN_COMMAND_2	0x3C	2	Allows system to request fans in the power supply to be set to the defined duty cycle. The system cannot cause the power supply fan to run slower than the power supply needs for cooling. This data should be in linear format. Example (32h=50% duty, 64h=100% Duty)	0xE0
IOUT_OC_WARN	0x4A	2	Used to support testing IOUT Overcurrent	0xE0
OT_WARN_LIMIT	0x51	2	Used to support testing CLST	0xE0
STATUS_BYTE	0x78	1	command to report the On/off status of the power supply. Please refer to page 72 of PMBus spec part 2	0xA0
STATUS_WORD	0x79	2	command to report the 2byte status of the power supply. Please refer to page 74 of PMBus spec part 2	0xA0
STATUS_VOUT	0x7A	1	command to report the output voltage status	0xE0
STATUS_IOUT	0x7B	1	command to report the output current status	0xE0
STATUS_INPUT	0x7C	1	command to report the input voltage and current status	0xE0
STATUS_TEMPERATURE	0x7D	1	command to report the device temperature status	0xE0
STATUS_CML	0x7E	1	command to report the device communication status	0xE0
STATUS_FANS_1_2	0x81	1	command to report the fan status	0xE0
READ_EIN	0x86	6 with block read	Command to report the accumulated input power (Total power usage since AC on)	0xAC

READ_EOUT	0x87	6 with block read	Command to report the accumulated output power (Total power usage since AC on)	0xAC

READ_VIN	0x88	2	RMS input voltage in volts(note; not used on power distribution boards) Should reset to 0 when AC is lost	0xA0
READ_IIN	0x89	2	RMS input current in amps (note; not used on power distribution boards) Should report 0 when AC is lost or in standby	0xA0
READ VOUT	0x8B	2	12V Output Voltage (should reset to 0 during standby or AC is removed)	0xA0
READ IOUT	0x8C	2	12V Output Current (should reset to 0 during standby or AC is removed)	0xA0
READ_TEMPERATURE1 (Ambient)	0x8D	2	Read airflow inlet temperature (should be similar to the ambient temperature)	0xA0
READ_TEMPERATURE2 (hot Spot)	0x8E	2	Read hotspot temperature (should be the hottest location inside the unit)	0xA0
READ_FAN_SPEED_1	0x90	2	Returns the fan speed in RPM of fan sensor 1. This data should be in linear format	0xA0
READ_FAN_SPEED_2	0x91	2	Returns the fan speed in RPM of fan sensor 2. This data should be in linear format	0xA0
READ POUT	0x96	2	12V DC Output in Watts	0xA0
READ PIN	0x97	2	AC input power in watts (note; not used on power distribution boards). Value should reset to 0W when in standby mode or AC is lost.	0xA0
PMBUS_REVISION	0x98	1	Reads the revision of the PMBus to which the device is compliant (default value 22h)	0xA0
APP_PROFILE_SUPPORT	0x9F	2 with block read	Defines that the power supply supports this application profile (default profile 05h), profile revision 1.0, (default revision value 10h)	0xA0
MFR_VIN_MIN	0xA0	2	Retrieves the minimum rated value, in volts, of input voltage (ex. 90Vac). This value remains a constant value.	0xA0
MFR_VIN_MAX	0xA1	2	Retrieves the maximum rated value, in volts, of input voltage (ex. 264Vac). This value is a constant value.	0xA0
MFR_PIN_MAX	0xA3	2	Retrieves the maximum rated value, in watts, of input power. If there is a high line or low line input power difference, the suitable input max power should be displayed properly. (ex. Power supply with rating 1000W@100-140Vac, 1200W@180-240Vac. During 100-140Vac, MFR_PIN_MAX=(1000W+10W fan DC power)/0.88 efficiency= 1148W. During 180-240Vac, MFR_PIN_MAX=(1200W+10W fan DC power)/0.9 efficiency=1345W)	0xA0
MFR_IOUT_MAX	0xA6	2	Retrieves the maximum rated 12V output current	0xA0

MFR_POUT_MAX	0xA7	2	Retrieves the maximum rated value, in watts, of output power. If there is a high line or low line input power difference, the suitable input max power should be displayed properly. (ex. Power supply with rating 1000W@100-140Vac, 1200W@180-240Vac. MFR_POUT_MAX should display 1000W or 1200W according to Vac input.	0xA0
MFR_TAMBIENT_MAX	0xA8	2	Retrieves the maximum rated ambient temperature, in degree C, in which the unit might be operated. This value is a constant value. (default 50 Degree C)	0xA0
MFR_TAMBIENT_MIN	0xA9	2	Retrieves the minimum rated ambient temperature, in degree C, in which the unit might be operated. This value is a constant value. (Default 0 Degree C)	0xA0
MFR_MAX_TEMP_1 (Ambient)	0xC0	2	This defines the maximum inlet temperature to generate a warning condition in the STATUS_TEMPERATURE command. This value is a constant value. Default value 50 Degree C.	0xA0
MFR_MAX_TEMP_2 (hot spot)	0xC1	2	This is the trip threshold for the hotspot temperature sensor (TEMP2) to asset SMBAlert#. This defines the maximum hotspot temperature to generate a warning condition in the STATUS_TEMPERATURE command. This value is a constant value. Default value setting: over temperature point minus 4 degree C.	0xA0

PAGE command definition:

The page command provides the ability to configure, control and monitor through only one physical address.

Each PAGES contains the operating memory. Each page may offer the full range of PMBus commands available for each output or non-PMBus device.

The data byte for the PAGE command is an unsigned binary integer.

Setting the page to FFh means that all following commands are to be applied to all memories.

The default value for PAGE is FFh.

CLEAR_FAULTS Command definition:

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device negates (clear, releases) its SMBALERT# signal output if the device is asserting the SMBALERT# signal.

The CLEAR_FAULTS does not cause a unit that has latched off for a fault condition to restart. Units that have shut

down for a fault condition are restarted by either power cycling or PSON toggling.

If the fault is still present when the bit is cleared, the fault bit shall immediately be set again and the host notified by the usual means.

This command is write only. There is no data byte for this command.

This will clear and reset all the fault and warning status bits to '0' at a given PAGE.

When the PAGE is set to FFh; all STATUS bits in all PAGEs shall be cleared by CLEAR_FAULTS command.

CAPABILITY Command Definition:

Table 7. CAPABILITY COMMAND Data Byte Format

Bits	Description	Value	Meaning
7	Packet Error Checking	0	Packet Error Checking not supported
		1	Packet Error Checking is supported
6:5	Maximum Bus Speed	00	Maximum supported bus speed is 100 kHz
		01	Maximum supported bus speed is 400 kHz
		10	Reserved
		11	Reserved
4	SMBALERT#	0	The device does not have a SMBALERT# pin and does not support the SMBus Alert Response protocol
		1	The device does have a SMBALERT# pin and does support the SMBus Alert Response protocol

CAPABILITY default value:

Bits	Description	Value	Meaning
7	Packet Error Checking	1	Packet Error Checking is supported
6:5	Maximum Bus Speed	00	Maximum supported bus speed is 100 kHz

4	SMBALERT#	1	0= The device does not have a SMBALERT# pin and does not support the SMBus Alert Response protocol 1= It has SMBALERT#
3:0	Reserved	0000	reserved

QUERY Command Definition:

The QUERY command is used to ask a PMBus device if it supports a given command, and if so, what data formats it supports for that command. This command uses the Block Write-Block Read Process Call described in the SMBus specification, Version 2.0.

For the write portion of the process call, the one data byte is an unsigned binary integer, the value of which is equal to the command code requested to be investigated.

For the read portion of the process call, the one data byte is an unsigned binary integer with values as the following table.

QUERY Command Returned Data Byte Format

Bits	Value	Meaning
7	1	Command is supported
	0	Command is not supported
6	1	Command is supported for write
	0	Command is not supported for write
5	1	Command is supported for read
	0	Command is not supported for read
4:2	000	Linear Data Format used
	011	Direct Mode Format used
	101	VID Mode Format used
	110	Manufacturer specific format used
1:0	XXX	Reserved for future use

If bit [7] is zero, then the rest of the bits are “don’t care”.

Without PEC block write – block read:

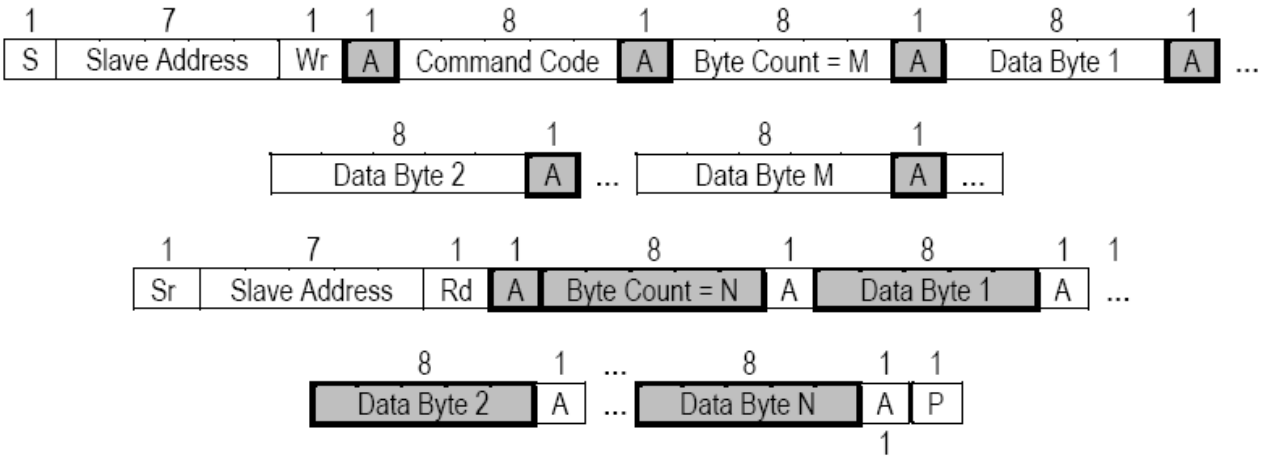


Figure 5-21: Block Write - Block Read Process Call

With PEC block write – block read:

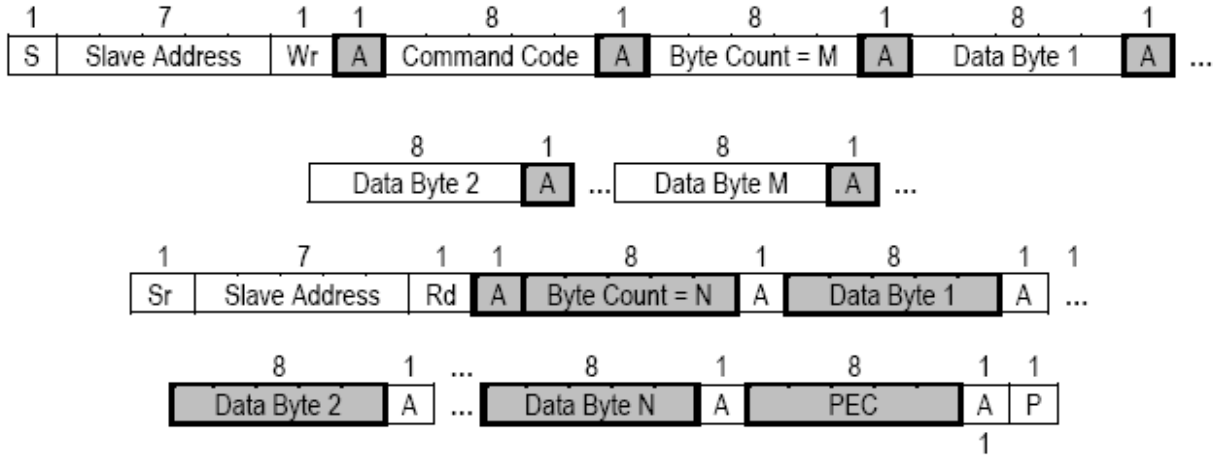


Figure 5-22: Block Write - Block Read Process Call with PEC

SMBALERT_MASK Command Definition:

The command format used to block a status bits from causing the SMBALERT# signal to be asserted. The bits in the mask byte align with the bits in the corresponding status register. For example, if the STATUS_TEMPERATURE command code were sent with mask byte 01000000b, then an Over temperature warning condition would be blocked from asserting SMBALERT#.

STATUS_WORD and STATUS_BYTE are not used with SMBALERT_MASK. The SMBALERT_Mask for

STATUS_WORD and STATUS_BYTE are not user changeable and retain the default value “1” (masked out) for all bits.

SMBALERT_MASK command can be used with any of the supported STATUS events. The events are masked from asserting SMBAlert# by writing a '1' to associated STATUS bits. The SMBALERT_MASK command is used in conjunction with the PAGE_PLUS command and the STATUS_commands. Below are the protocols.

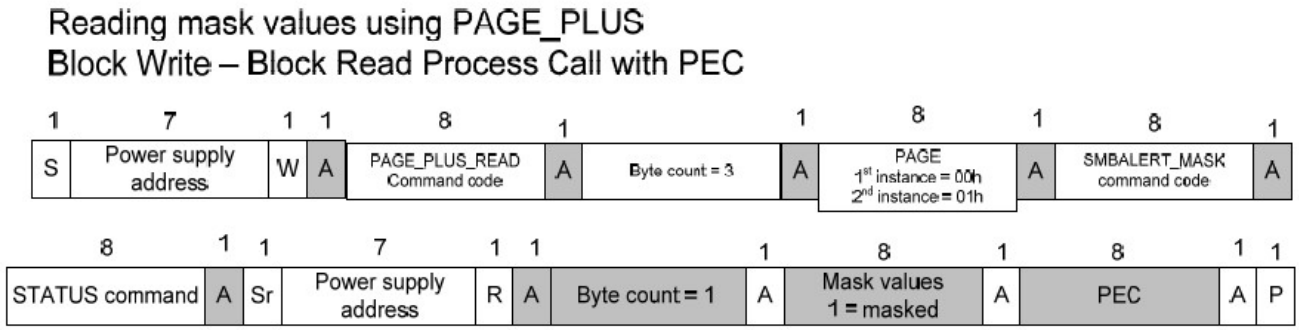
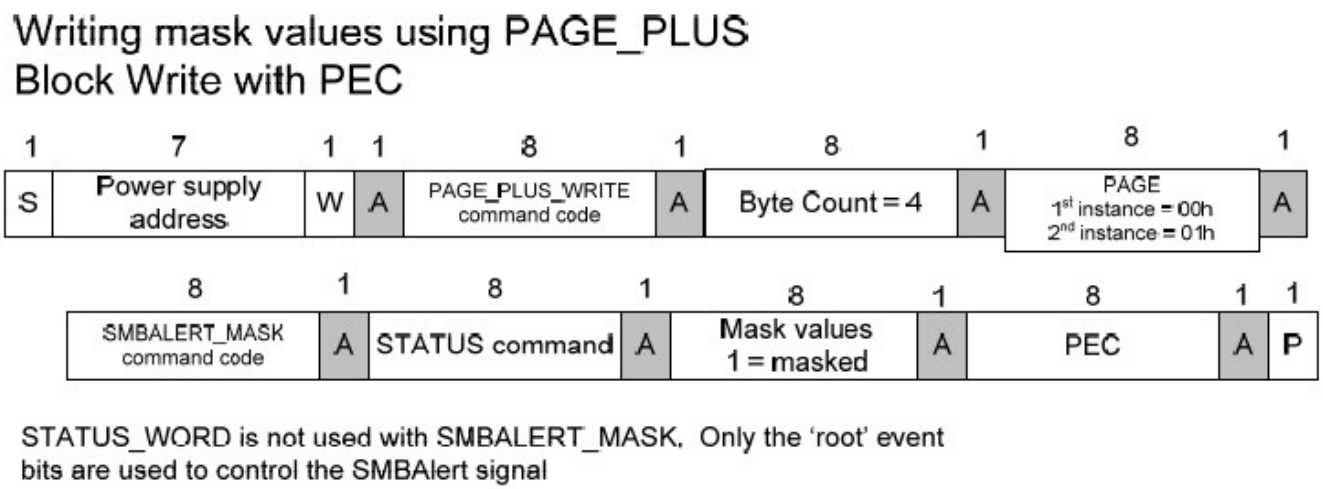


Figure 5 PAGE_PLUS_READ command.



STATUS_WORD is not used with SMBALERT_MASK. Only the 'root' event bits are used to control the SMBAlert signal

Figure 6 PAGE_PLUS_WRITE command.

VOUT_MODE Command Definition:

For reading output voltages the power supply shall support the VOUT_MODE command to report the output voltage formatting for the READ_VOUT command. The VOUT_MODE shall be set to Linear and the exponent (N) shall be set to -9.

VOUT_MODE settings for reading output voltage(s).

Mode	Bits [7:5]	Bits [4:0] (N)

Linear	000b	10111b (-9)

COEFFICIENT Command Definition:

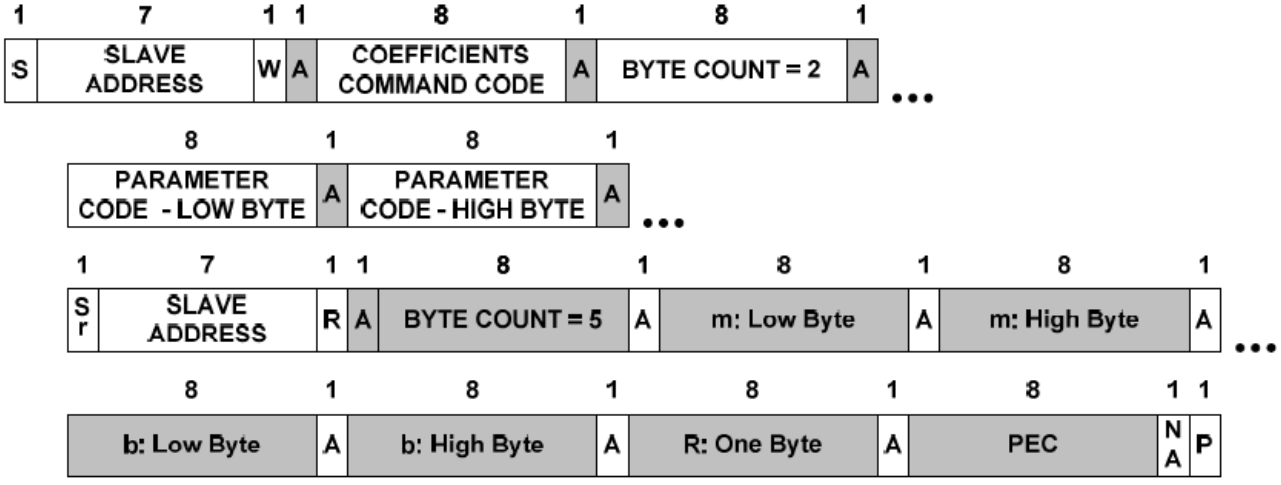
The system shall use this to read the values of m, b, and R used to determine READ_EIN accumulated power values. This command uses the Block Write-Block Read Process Call described in the SMBus specification, Version 2.0.

For the write portion of the process call, the byte count is two and there are two data bytes. The first data byte is the command of interest (ex. 0x86 for READ_EIN and 0x87 for READ_EOUT). The second data byte indicates whether the host requesting the coefficients needed to encode a value to be written to the device or the coefficients needed to decode a value read from the device. A value of 01h in the second data byte indicates that the coefficients needed to decode a value read from the device are being requested. A value of 00h in the second byte indicates that the coefficients needed to encode a value for writing are being requested.

For the read portion of the process call, the byte count is five and the five bytes returned are (in this order):

1) Lower byte of m,
2) Upper byte of m,
3) Lower byte of b
4) Upper byte of b,
5) Single byte of R.

More information on the function and application of this command are given in Section 7.2. An example of the packet construction for retrieving the coefficients from a PMBus device using PEC is shown below.



Retrieving Coefficients Using PEC

The default values of m, b, and R shall be set to:

m=0001h

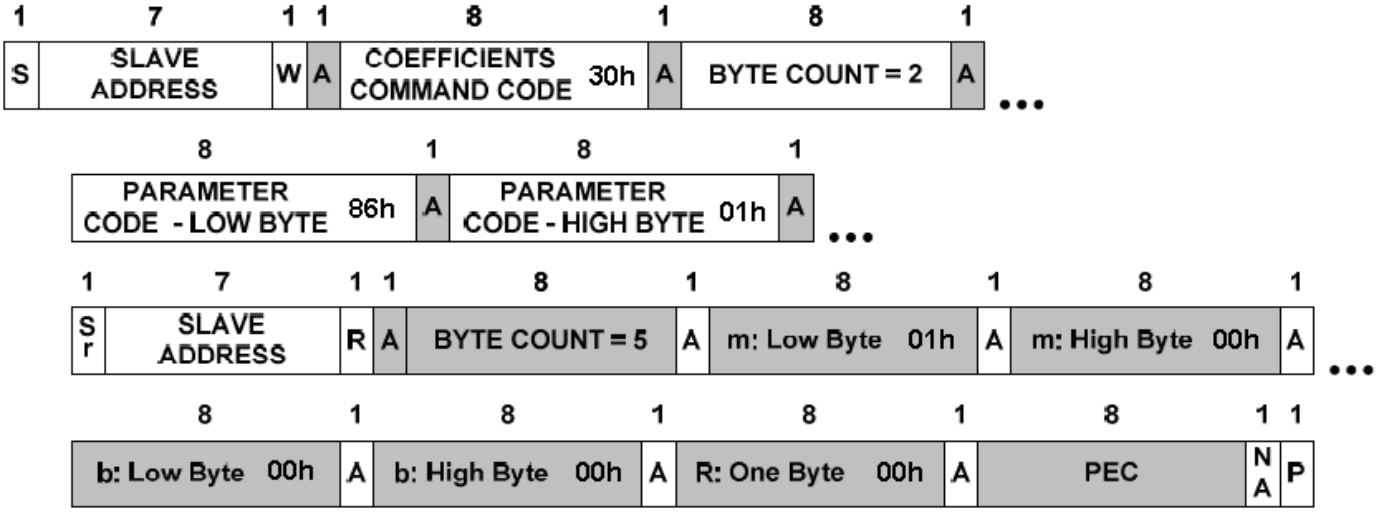
b=0000h

R=00h

Table 8 PSU PMBus COEFFICIENTS Command

Command	COEFFICIENTS support	m	B	R
READ_EIN	Yes	01h	00h	00h
READ_EOUT	Yes	01h	00h	00h

Example for obtaining the coefficient for READ_EIN with default values:



FAN_CONFIG_1_2 Command Definition:

Bit(s)	Default Value	Meaning
7	1	Fan 1 presence, 0=no fan1, 1=fan1 installed
6	0	Fan 1 commanded in RPM=1, commanded in duty cycle=0; Default is 0x0=duty command
5:4	0	Not used
3	1 or 0	Fan 2 presence, 0=no fan2, 1=fan2 installed
2	0	Fan 2 commanded in RPM=1, commanded in duty cycle=0; Default is 0=duty command
1:0	0	Not used

FAN_COMMAND_1_2 Command Definition:

The system may increase the power supplies fan speed through using the FAN_COMMAND Command. This command can only increase the power supply fan speed; it cannot decrease the power supply fan speed below what the power supply commands.

The control is configured to be duty cycle controlled using the linear format of the PMBus protocol.

The exponent N is fixed to a value of 0 (N=0). The command ranges from value 0000h (0% duty) to 0064h (100% duty).

IOUT_OC_WARN_LIMIT Command Definition:

The IOUT_OC+WARN_LIMIT command sets the value of the output current that causes an output overcurrent warning. The two data bytes are formatted in Linear Data format. In response to the IOUT_WARN_LIMIT being exceeded, the device should:

- Sets the OTHER_FAULT bit (bit0) in the STATUS_BYTE
- Sets the IOUT fault/warning bit (bit6) in the STATUS_WORD
- Sets the IOUT_OC_WARNING bit (bit5) in the STATUS_IOUT register

OT_WARN_LIMIT Command Definition:

The OT_WARN_LIMIT command set the temperature, in degrees Celsius, of the unit at which it should indicate an Overtemperature Warning Alarm. The two data bytes are formatted in the Linear Data Format.
In response to the OT_WARN_LIMIT being exceeded, the device should:

- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the OT_WARNING bit in the STATUS_TEMPERATURE register

STATUS Commands:

The following PMBus STATUS commands shall be supported. All STATUS commands except the STATUS_FAN_1_2 and STATUS_BYTE commands shall be accessed with the PAGE_PLUS command since they are used by both the BMC and ME. The (BMC) and (ME) refer to the two instances of the command accessed via the PAGE_PLUS command. The status bits shall assert whenever the event driving the status bit is present. Once a bit is asserted it shall stay asserted until cleared using one of the five methods described below:

1) Writing a '1' to any given bit location shall reset on that bit of the command
2) Sending a CLEAR_FAULTS command to the power supply shall reset all STATUS_ bits to '0' at a given PAGE. If the PAGE is set to FFh; all STATUS bits in all PAGEs shall be cleared.
3) Cycling input power OFF(when Vin below 90Vac) than ON (when Vin above 90Vac) shall reset all STATUS_ bits to '0'.
4) Systems with redundant power supplies where only one of the supplies cycle AC power OFF/ON; the power cycled power supply shall reset the STATUS_ bits to '0' only when powered back ON. If the power supply is kept OFF, the STATUS_ bits shall not be reset.
5) Cycling the PSON# signal from de-asserted to asserted shall reset the STATUS_ bits to '0'. The bits shall

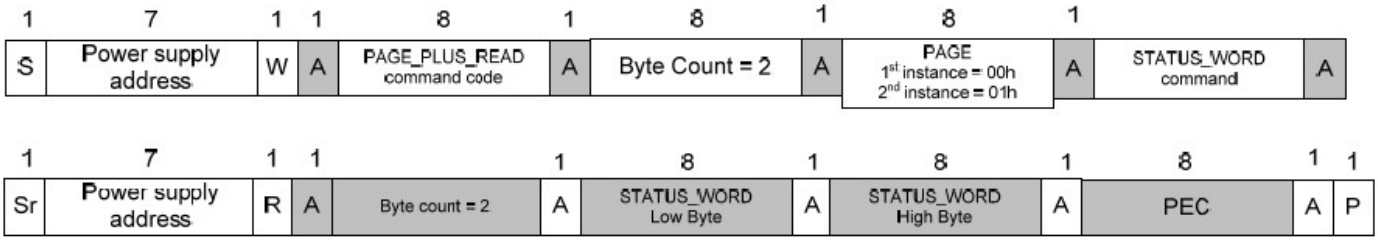
be reset only on the assertion of PSON#; not the de-assertion.

The STATUS commands that are supported with PAGE_PLUS_READ and PAGE_PLUS_WRITE commands shall still support direct access of the base STATUS_XXX commands using read word, write word, read byte, and write byte protocols.

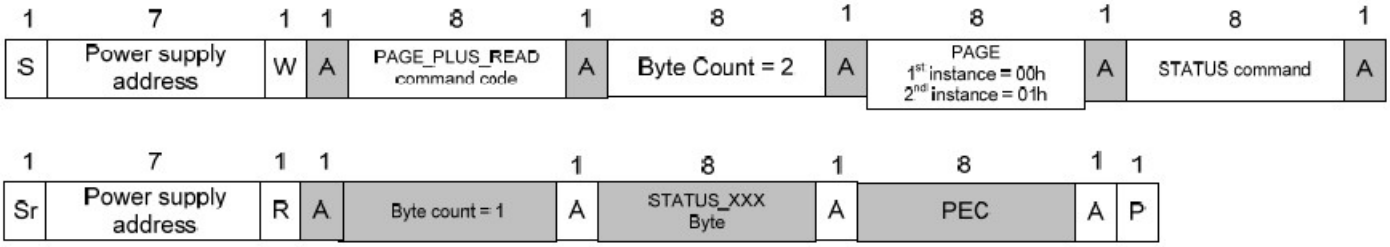
STATUS_FAN_1_2 command is only accessed by the system BMC. It uses standard read byte protocol to read status and write byte protocol to clear bits.

Example for STATUS_WORD using PAGE_PLUS_READ for read access:

Reading STATUS_WORD
Block Write – Block Read Process Call with PEC

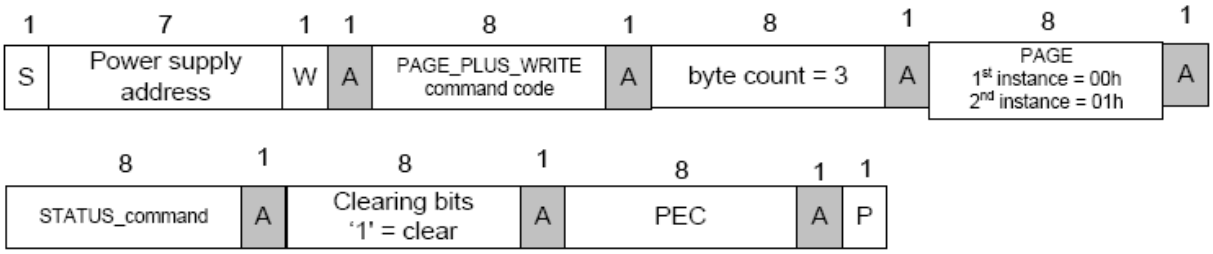


Reading STATUS_TEMPERATURE, STATUS_IOUT, STATUS_INPUT, STATUS_CML
Block Write – Block Read Process Call with PEC



Clearing STATUS command bit example:

Clearing STATUS commands (write '1' to clear a bit)
STATUS_TEMPERATURE, STATUS_IOUT, STATUS_INPUT, STATUS_CML
Block Write with PEC



STATUS_WORD cannot be cleared directly It is cleared based on lower level status commands

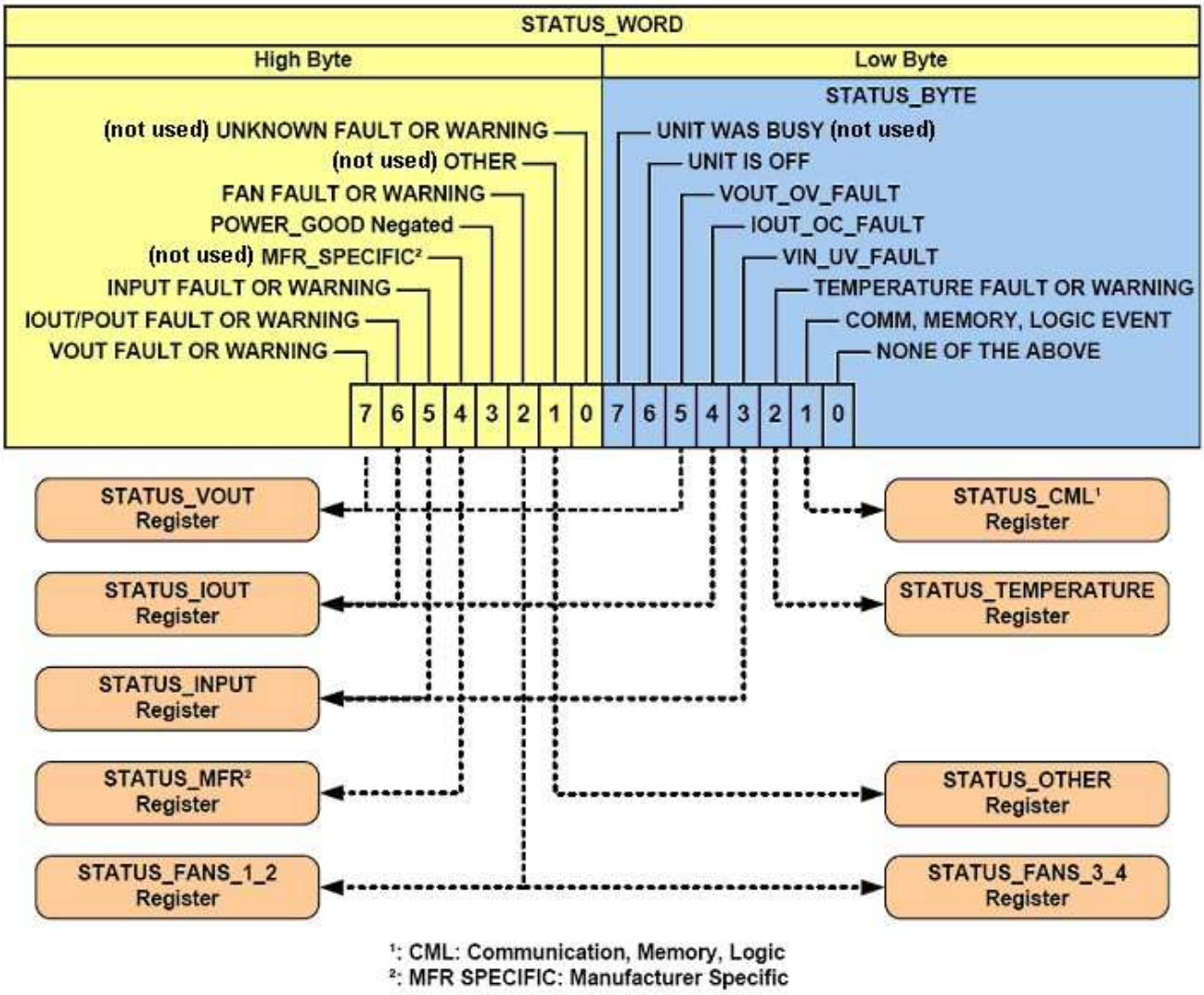
STATUS_BYTE: Please refer to PMBus part 2 spec page 72.

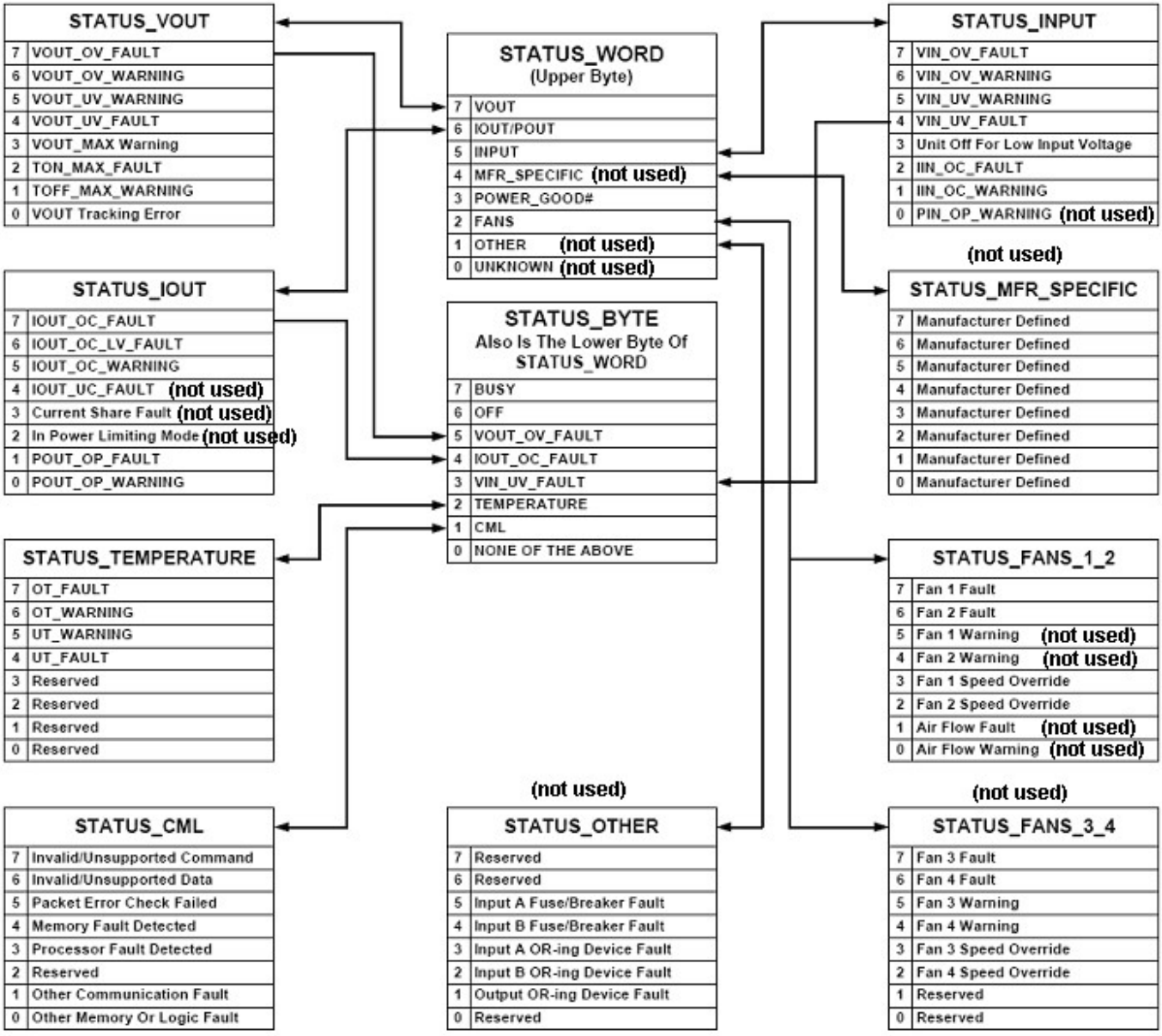
Offset 0x78			Instances: Without PAGE'ing PAGE 00h=BMC PAGE 01h=ME	SMBAlert_Mask defaults for each of the three instances (NO PAGE'ing, PAGE 00h, PAGE 01h) 0 = causes assertion of SMBalert# 1= does not cause assertion of SMBAlert#
Bit #	7	Not used, default=0	Without PAGE'ing, 00h, 01h	NA
	6	Device is off due to PSON or for any reason (ex. Protection)=1, else 0		NA
	5	Output OVP fault=1, else 0		NA
	4	Output OCP fault =1, else 0		NA
	3	Vin under voltage fault =1, else 0 (must be detected within 2ms)		NA
	2	Temperature fault or warning occur=1; else 0;		NA
	1	CML communication error=1, else 0		NA
	0	Other fault (A fault or warning not listed in bit [7:1] of this byte has occurred)=1, else=0		NA

STATUS_WORD: Please refer to PMBus part 2 spec page 74.

Byte	STATUS_WORD, Offset 0x79		Instances: Without PAGE'ing PAGE 00h=BMC PAGE 01h=ME	SMBAlert_Mask defaults for each of the three instances (NO PAGE'ing, PAGE 00h, PAGE 01h) 0 = causes assertion of SMBalert# 1= does not cause assertion of SMBAlert#
Low	7	Not used, default=0	Without PAGE'ing, 00h, 01h	NA
	6	Device is off due to PSON or for any reason (ex. Protection)=1, else 0		NA
	5	Output OVP fault occur=1, else 0		NA
	4	Output OCP fault occur =1, else 0		NA
	3	Vin under voltage fault occur =1, else 0 (must be detected within 2ms)		NA
	2	Temperature fault or warning occur=1; else 0		NA
	1	CML communication error=1, else 0		NA
	0	Other Fault (A fault or warning not listed in bit [7:1] of this byte has occurred)=1, else=0		NA
High	7	VOUT Fault or warning=1, else 0		NA
	6	IOUT/POUT fault or warning=1, else 0		NA
	5	An input voltage, input current, or input power fault or warning=1, else 0		NA
	4	Not used, default=0		NA

	3	Power Good signal is not good (logic low)=1, else 0		NA
	2	Fan fault or warning=1, else 0		NA
	1	Not used, default=0		NA
	0	Not used, default=0		NA





STATUS_VOUT Command Definition:

Bit	STATUS_VOUT, Offset 0x7A	Instances: Without PAGE'ing PAGE 00h=BMC PAGE 01h=ME		SMBAlert_Mask defaults for each of the three instances (NO PAGE'ing, PAGE 00h, PAGE 01h) 0 = causes assertion of SMBalert# 1= does not cause assertion of SMBAlert#

7	VOUT over voltage fault	No PAGE'ing	1 , NA, NA

6	Not used, default=0		1 , NA, NA
5	Not used, default=0		1 , NA, NA
4	VOUT under voltage fault		1 , NA, NA
3	Not used, default=0		1 , NA, NA
2	Not used, default=0		1 , NA, NA
1	Not used, default=0		1 , NA, NA
0	Not used, default=0		1 , NA, NA

STATUS_IOUT Command Definition:

Bit	STATUS_IOUT, Offset 0x7B	Instances: Without PAGE'ing PAGE 00h=BMC PAGE 01h=ME	SMBAlert_Mask defaults for each of the three instances (NO PAGE'ing, PAGE 00h, PAGE 01h) 0 = causes assertion of SMBalert# 1= does not cause assertion of SMBAlert#
7	IOUT Overcurrent Fault	Without PAGE'ing, 00h, 01h	1, 1, 1
6	Not used, default=0		1, 1, 1
5	IOUT Overcurrent Warning (greater than rated output current for more than 1second)		1. 1. 0
4	Not used, default=0		1, 1, 1
3	Not used, default=0		1, 1, 1
2	Not used, default=0		1, 1, 1
1	POUT Overpower Fault		1, 1, 1
0	POUT Overpower Warning (greater than rated output power for more than 1 second)		1, 1, 1

STATUS_INPUT Command Definition:

Bit	STATUS_INPUT, Offset 0x7C	Instances: Without PAGE'ing PAGE 00h=BMC PAGE 01h=ME	SMBAlert_Mask defaults for each of the three instances (NO PAGE'ing, PAGE 00h, PAGE 01h) 0 = causes assertion of SMBalert# 1= does not cause assertion of SMBAlert#
7	Not used, default=0;	Without PAGE'ing, 00h, 01h	1, 1, 1
6	Not used, default=0;		1, 1, 1
5	Vin Under voltage Warning (Vin<88Vac)		1, 1, 1

4	Vin Under voltage Fault (Condition of Vin< 80Vac. When Vin<10Vac, event must be detected within 2ms)		1, 1, 0

3	Unit is off for insufficient Input Voltage (Input UVP)		1, 1, 1
2	IIN Over current Fault (When unit is shut down due to input over current)		1, 1, 1
1	IIN Over current Warning (When IIN over IO label input current max rating for more than 1 second)		1, 1, 1
0	Not used, default=0;		1, 1, 1

STATUS_TEMPERATURE Command Definition:

Bit	STATUS_TEMPERATURE, Offset 0x7D	Instances: Without PAGE'ing PAGE 00h=BMC PAGE 01h=ME	SMBAlert_Mask defaults for each of the three instances (NO PAGE'ing, PAGE 00h, PAGE 01h) 0 = causes assertion of SMBalert# 1= does not cause assertion of SMBAlert#
7	Overtemperature Fault (When Over temperature protection is triggered)	Without PAGE'ing, 00h, 01h	1, 1, 1
6	Overtemperature Warning (When READ_TEMPERATURE2 exceed MFR_MAX_TEMP_2)		1, 1, 0
5	Not used, default=0;		1, 1, 1
4	Not used, default=0;		1, 1, 1
3	Not used, default=0;		1, 1, 1
2	Not used, default=0;		1, 1, 1
1	Not used, default=0;		1, 1, 1
0	Not used, default=0;		1, 1, 1

STATUS_CML Command Definition:

Bit	STATUS_CML, Offset 0x7E	Instances: Without PAGE'ing PAGE 00h=BMC PAGE 01h=ME	SMBAlert_Mask defaults for each of the three instances (NO PAGE'ing, PAGE 00h, PAGE 01h) 0 = causes assertion of SMBalert# 1= does not cause assertion of SMBAlert#
7	Invalid/Unsupported Command received =1, else 0;	No PAGE'ing	1 , NA, NA
6	Not used, default=0		1 , NA, NA
5	Packet Error Check(PEC) failed=1; else 0;		1 , NA, NA
4	Not used, default=0		1 , NA, NA
3	Not used, default=0		1 , NA, NA

2	Not used, default=0	1 , NA, NA

1	Other Communication Fault(ex. Missing bit), =1; else 0;		1 , NA, NA
0	Not used, default=0		1 , NA, NA

STATUS_FANS_1_2 Command Definition:

Bit	STATUS_FANS_1_2, Offset 0x81	Instances: Without PAGE'ing PAGE 00h=BMC PAGE 01h=ME	SMBAlert_Mask defaults for each of the three instances (NO PAGE'ing, PAGE 00h, PAGE 01h) 0 = causes assertion of SMBalert# 1= does not cause assertion of SMBAlert#
7	Fan (either fan1 or fan 2) Fault=1, else=0 All fans in the PSU shall be OR'ed into a single fan status bit for fault conditions	No PAGE'ing	1 , NA, NA
6	Not used, default=0;		1 , NA, NA
5	Not used, default=0;		1 , NA, NA
4	Not used, default=0;		1 , NA, NA
3	Fan 1 Speed Overridden (When User command is applied)=1; else 0		1 , NA, NA
2	Fan 2 Speed Overridden (When User command is applied)=1; else 0		1 , NA, NA
1	Not used, default=0;		1 , NA, NA
0	Not used, default=0;		1 , NA, NA

READ_EIN & READ_EOUT Command Definition:

The READ_EIN & READ_EOUT command shall use the PMBus direct format to report the accumulated power value and the sample count. The PMBus coefficients m, R, and B shall be fixed values and the power supply shall report these values using the PMBus COEFFICIENT command. The coefficient m shall be set to 01h, coefficient R shall be set to 00h, and coefficient b shall be set to 00h.

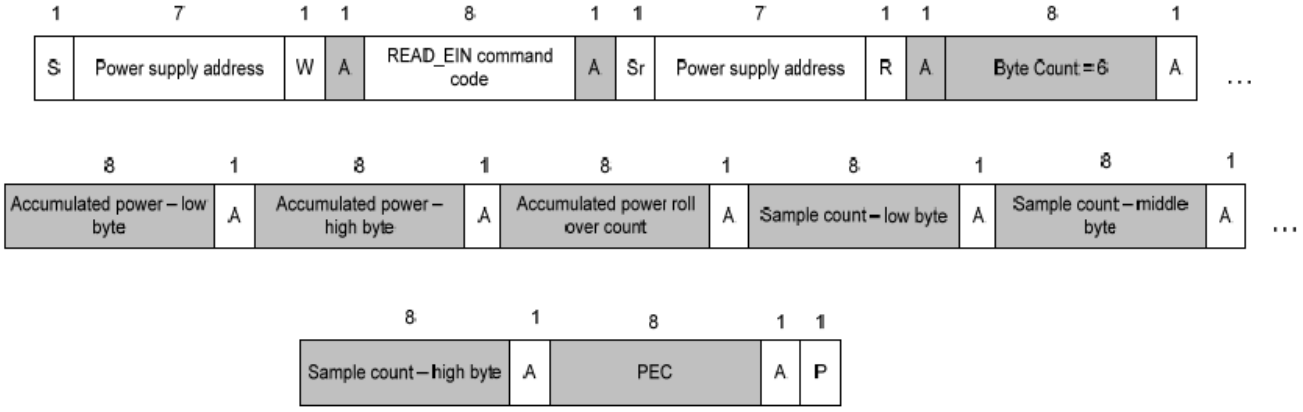
Table 3 READ_EIN Requirements Summary

	MIN	MAX	Description
Format	PMBus Direct format m = 01h, R = 00h, b = 00h		PMBus data format; refer to PMBus specification for details.
P_{sample} averaging period	= 4 AC cycles		Period instantaneous AC power is averaged over to calculate P_{sample}.
[P_{accum} / N] Accuracy (10% to 200W load)	+/-10W		The calculated input power data shall meet these accuracy requirements over 100-240VAC and under the defined system polling rate.
[P_{accum} / N] Accuracy (200W to 100% load)	+/-5%		
System polling rate	1 sample / sec	10 samples / sec	The power supply shall be polled over this range of rates while testing accuracy.

Table 7 READ_EOUT Requirements Summary

	MIN	MAX	Description
Format	PMBus Direct format m = 01h, R = 00h, b = 00h		PMBus data format; refer to PMBus specification for details.
P_{sample} averaging period	~50ms		Period instantaneous input power is averaged over to calculate P_{sample}.
Sampling period	10ms	50ms	Period at which the power accumulator and sample counter are updated
[P_{accum} / N] Accuracy (5% to 100% load)	±2% to ±5%		The calculated input power data shall meet these accuracy requirements over 100-240VAC (-36VDC to -75VDC for DC input power supplies) and under the defined system polling rate.
System polling rate	1 sample /s	10 samples /s	The PSU shall be polled over this range of rates while testing accuracy.

READ_EIN and READ_EOUT shall use the SMBus block Read with PEC protocol in the below format:

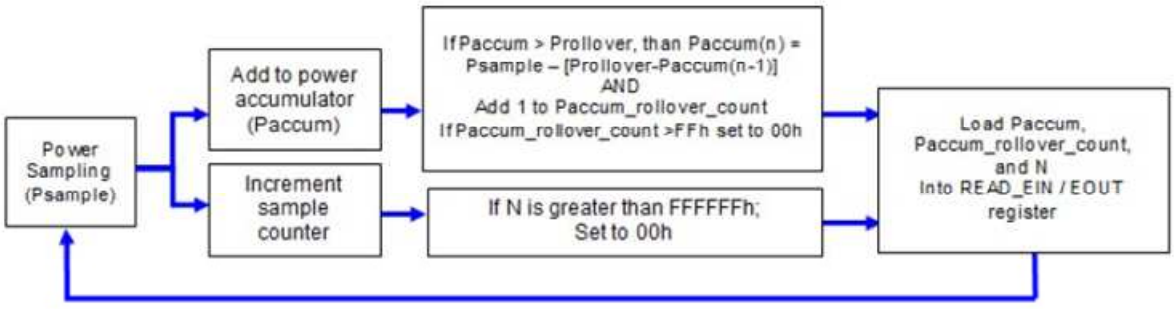


READ_EIN Command

READ_EIN and READ_EOUT Accumulators:

The accumulated power data shall be the sum of input power values averaged over 4 AC cycles (or over 50ms for READ_EOUT). The value shall automatically roll-over when the 15bit maximum value is reached (>7FFFh). The sample count should increment 1 for each accumulated power value. The system shall calculate average power by dividing the accumulated power value by the sample count. The system must sample READ_EIN and READ_EOUT faster than the roll-over period to get an accurate power calculation. If the system sees a smaller value than the previous sampled data; then the system must account for the roll-over by adding 7FFFh to the present value. Below is a block diagram depicting the READ_EIN accumulator function in the power supply.

Important note: When the PSU responds to the system requesting READ_EIN or READ_EOUT data; the data in the sample count must always alignment with the number of samples accumulated in the power accumulator. To achieve this power accumulator, power rollover counter, and sample counter shall be loaded into a READ_EIN and READ_EOUT register at the same time.



Where:

Psample: The sampled power value in linear or direct format
Paccum: 2 bytes in PMBus linear or direct format. The accumulated power values made up of Psample(0) + Psample(1) + … + Psample(n)
N: 3 byte unsigned integer value. The number of accumulated power values summed in Paccum
Prollover: The max value of Paccum before a rollover will occur
Paccum_rollover_count: 1 byte unsigned integer counting the number of times Paccum rolls over. Once this reaches FFh; it will automatically get reset to 00h

Resetting READ_EIN and READ_EOUT:

The READ_EIN and READ_EOUT power accumulator, roll-over counter, and sample count should keep the latest value when the power supply is put into standby mode. The power accumulator, roll-over counter and sample count should reset to 00 when AC power is lost.

PMBUS_REVISION Command Value:

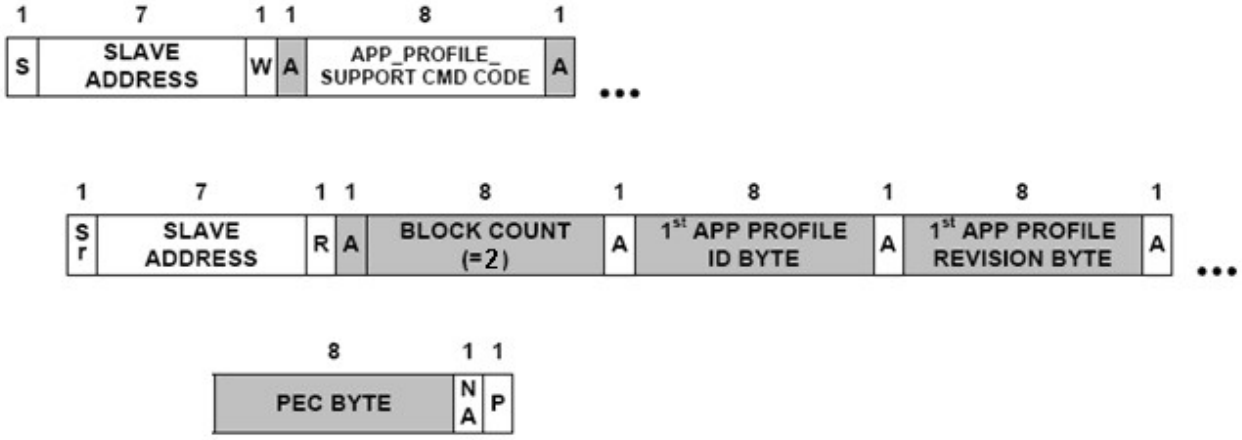
Bits 7:4	Part I Revision	Bits 3:0	Part II Revision
0010	1.2	0010	1.2

APP_PROFILE_SUPPORT Command:

The Block Read protocol is used with this command.

First Byte for supporting Grantley Profile: 05h

Second Byte for supporting Grantley Profile rev 1.0: 10h



12.6 Manufacturer Specific Commands

Offset 0xD0-0xDE is used to represent the unit model serial number. Data represented in byte format.

These bytes are read/write capable through I2C

Below serial number is for example only:

For CPS-5011-xAx TBD

	Serial number		
Offset	character	Hex	Query Command Response (Hex)
D0	TBD	50	
D1	TBD	35	
D2	TBD	30	
D3	TBD	35	
D4	TBD	50	
D5	TBD	41	
D6	TBD	45	
D7	TBD	30	
D8	TBD	31	
D9	TBD	41	
DA	TBD	30	
DB	TBD	30	
DC	TBD	30	
DD	TBD	30	
DE	TBD	31	

Offset 0xE0 – 0xEB is used to represent the model number, data represented in byte format. These bytes are read only capable through I2C.

For CPS-5011-xAx

	Item number		
Offset	character	Hex	Query Command Response (Hex)
E0	TBD		
E1	TBD		
E2	TBD		
E3	TBD		
E4	TBD		
E5	TBD		
E6	TBD		
E7	TBD		
E8	TBD		
E9	TBD		
EA	TBD		
EB		00 (end of field)	
EC		00 (end of field)	

Additional information bytes for FRU backward compatibility. These bytes are read only capable.

Offset	Function	Description
ED	Temperature upper limit	Internal temperature upper limit in degree Celsius. Direct data format, data length is one byte.
EE	Fan 1 pulse count lower limit	Value to represent the lower limit RPM of the power supply fan #1 The system software will convert this value, to fan RPM, using: RPM limit=(1/0.262) *(Fan Pulse Count limit * 60 /2)
EF	Fan 2 pulse count lower limit	Same calculation as fan 1. If fan 2 is not available, default value is 0x00.

Offset 0xF0-0xF5 is used to represent the unit revision number. Revision begins with Rev 1.0. Data is represented in byte format. These bytes are read only capable using I2C.

	Revision		
Offset	character	Hex	Query Command Response (hex)
F0	TBD		B8
F1	TBD		B8
F2	TBD		B8
F3	TBD		B8
F4	TBD		B8
F5	TBD		B8
F6		00 (End of field)	B8

12.7 Sensor Sampling

The sensor registers inside the power supply for monitoring input/output power, current, and voltage shall meet the following minimum requirements. Register refresh rate is the frequency the sensor register gets updated with a new measurement value.

Register refresh rate 10Hz

12.8 Sensor Averaging

The sensor registers for monitoring input/output power, current, voltage, fan speed, and temperature shall contained

averaged data, not instantaneous peak data. This may be achieved in two ways; an arithmetic average or a low pass filter. An exponential moving average shall not be used. The power supply shall refresh the sensor data at a rate no slower than the averaging duration.

READ_PIN, READ_POUT, READ_VOUT, READ_IOUT, READ_TEMPERATURE1, READ_TEMPERATURE2, READ_FAN_SPEED1 and READ_FAN_SPEED2 (if available) shall be an average value over a 2 to 10 second interval.

READ_IIN, and READ_VIN shall be an RMS value over a 2 second interval.

12.9 Accuracy

The sensor commands shall meet the following accuracy requirements.

	5% to 10% loading	10% loading to 200W input	200W input to 100% loading
READ_IIN	N/A	+/-5%	+/-3%
READ_PIN	+/-10W	+/-10W	+/-5%
READ_EIN	+/-10W	+/-10W	+/-5%
READ_EOUT	+/-10W	+/-10W	+/-5%
READ_IOUT	N/A	+/-5%	+/-3%
READ_POUT	+/-10W	+/-10W	+/-5%

READ_VIN	+/- 2% over full range
READ_VOUT	+/- 2% over full range
READ_TEMPERATURE	Required: +/-2 ℃ over full range
READ_FAN_SPEED 1 and 2	+/-10%

Table 2 READ_PIN Requirements Summary

	MIN	MAX	Description
Format	PMBus linear format		PMBus data format; refer to PMBus specification for details
Averaging period	2 sec	10 sec	The AC input power shall be averaged using a simple averaging method of a filtering method. This defines the max/min period for simple averaging and the bandwidth range if the filter method is used.
Filtering bandwidth	0.1 Hz	0.5 Hz	
Accuracy (10% to 200W load)	+/- 10W		The input power data shall meet these accuracy requirements over 100-240VAC and under the defined system polling rate.
Accuracy (200W to 100% load)	+/- 5%		
System polling rate	1 sample/ sec	10 samples / sec	The power supply shall be polled over this range of rates while testing accuracy.

Table 3 READ_EIN Requirements Summary

	MIN	MAX	Description
Format	PMBus Direct format m = 01h, R = 00h, b = 00h		PMBus data format; refer to PMBus specification for details.
P_{sample} averaging period	= 4 AC cycles		Period instantaneous AC power is averaged over to calculate P_{sample}.
[P_{accum} / N] Accuracy (10% to 200W load)	+/-10W		The calculated input power data shall meet these accuracy requirements over 100-240VAC and under the defined system polling rate.
[P_{accum} / N] Accuracy (200W to 100% load)	+/-5%		
System polling rate	1 sample / sec	10 samples / sec	The power supply shall be polled over this range of rates while testing accuracy.

12.10 Linearity

For any increase in actual power or current the resulting PMBus reading shall stay the same or increase. For any decrease in actual power or current the resulting PMBus reading shall stay the same or decrease.

12.11 Resolution

The resolution of the PMBus input power sensor shall be no more than 3W. With an increasing or decreasing load in 1W steps; the associated power change using READ_PIN shall not exceed 3W.

12.12 SMBAlert

The SMBAlert# Signal may be asserted (pulled low, less than 0.4V) by the power supply for any of the supported STATUS events. The events that control SMBAlert# can be masked during the SMBALERT_MASK command. Default masking is shown in section 20.2.E of the status command definitions.

By default the SMBAlert# signal is asserted for the following cases:

1) AC Input voltage drops below the fault threshold (<10Vac) for more than 1.8ms and must be detected within 2ms.
2) Thermal sensor on a hot spot inside the power supply has exceeded its warning temperature (MFR_MAX_TEMP2)
3) Power supply is turned off due to PSON

The power supply does not support Alert Response Address (ARA). After asserting the SMBAlert# signal, the power supply shall keep its address at its standard address; not change to 18h.

The SMBAlert# signal shall be asserted whenever any un-masked event has occurred. This is a level detected event. Whenever the event is present SMBAlert# shall be asserted. If the SMBAlert signal is cleared, it shall immediately

re-asserted if the event is still present.

The SMBAlert# signal shall be cleared and re-armed by the following methods:

1) Clearing STATUS bits causing the asserted SMBAlert# signal.
2) Power cycling with PSON or with AC power
3) Using CLEAR_FAULTS command that clears all fault
4) Cycling AC power OFF(when Vin below 90Vac) than ON (when Vin above 90Vac) shall reset the SMBAlert#
5) Systems with redundant power supplies where only one of the supplies cycle AC power OFF/ON; the power cycled power supply shall reset the SMBAlert# only when the device is powered back ON. If the power supply is kept OFF, the SMBAlert# shall not be reset.

During Standby mode or AC off (both single or redundant mode), SMBAlert# should be logic low (less than 0.4V) and be able to sink 4mA current.

SMBAlert# Logic Level

	MIN	**MAX**	**Nominal**
Logic level low voltage, Isink = 4mA	0V	0.4V	0V
Logic level high voltage, Isource = 200μA	2.4V	5.25V	5V

Figure 1: AC ON condition SMBAlert timing sequence

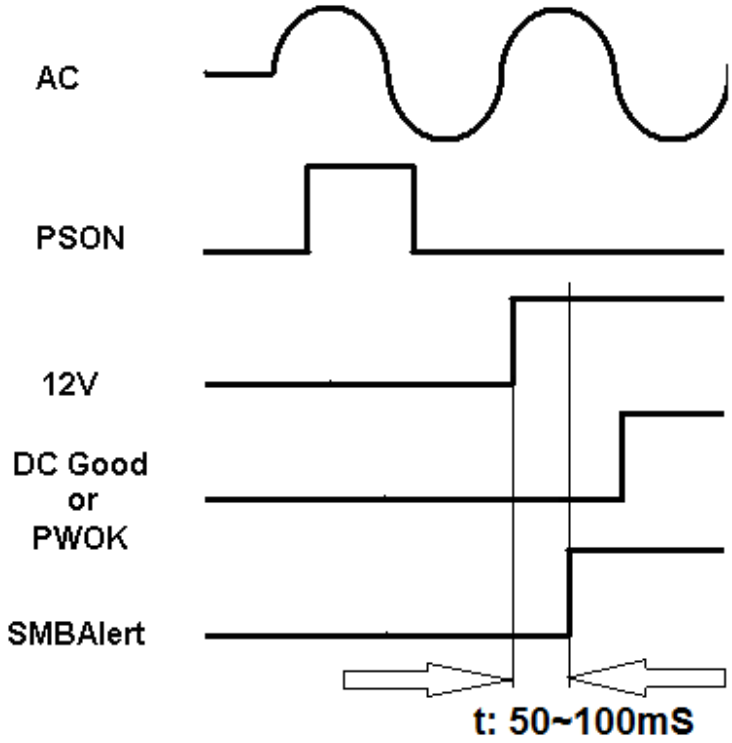


Figure 2: PSON=off power down condition (AC always ON) SMBAlert timing sequence

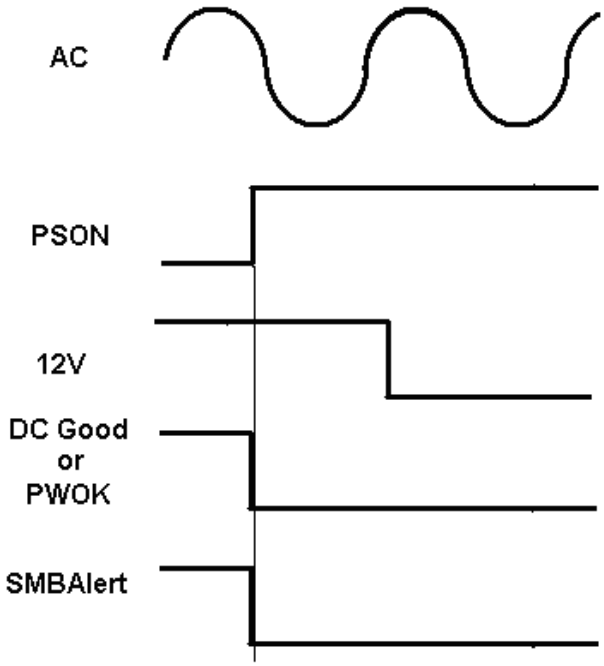


Figure 3: Power down condition due to AC OFF SMBAlert# timing sequence

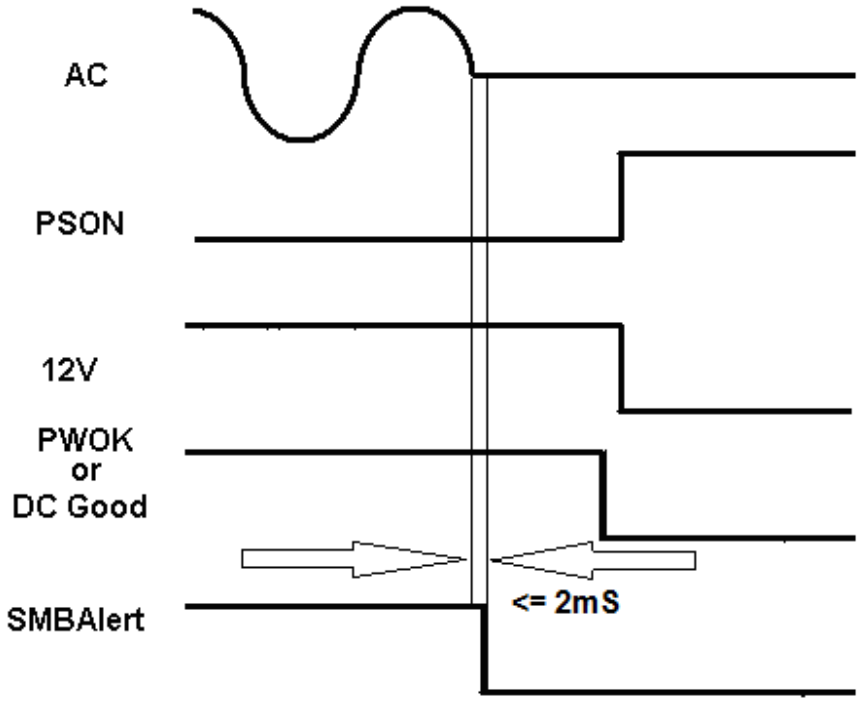
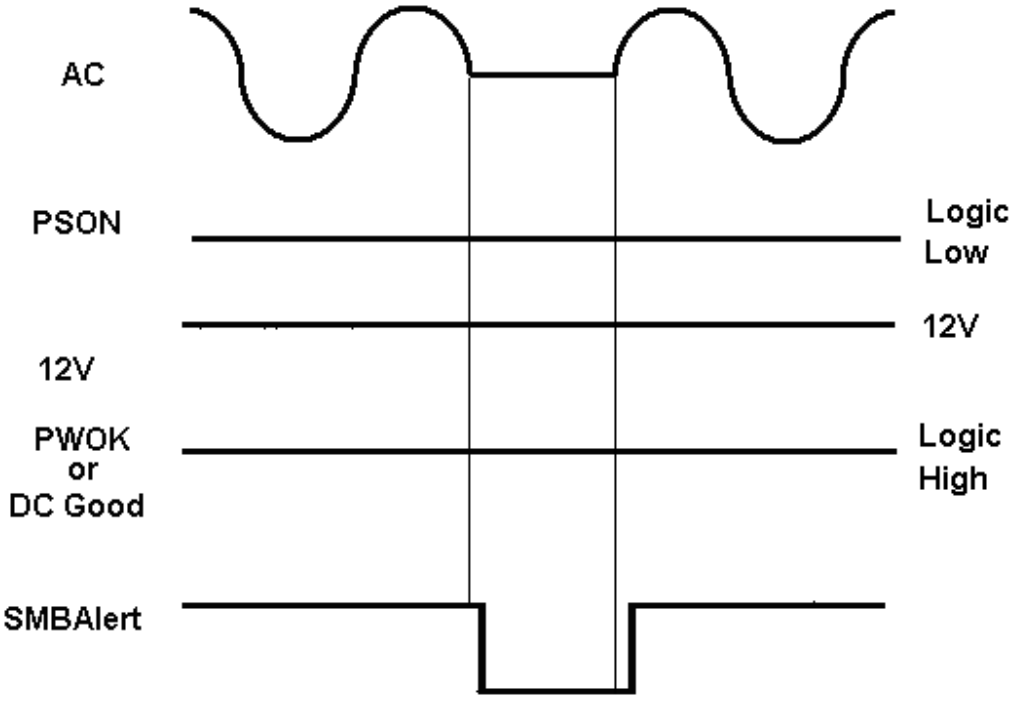


Figure 4: AC Loss within hold up time, SMBAlert will be triggered during AC Loss. SMBAlert will return to nominal after AC voltage is resumed.



12.13 Faults and Error Checking

The power supply shall support PEC(packet error checking) per the SMBus 2.0 specification.

The power supply shall also support and respond to commands which do not contain PEC (packet error checking).

12.14 Black Box Recording Function

The power supply will have a software black box feature which records the cause of an abnormal fault. The records are used with the I2C slave addresses (0x70, 0x72, 0x74, 0x76 depending on A1, A0 signals accordingly).

The below error codes will be stored in the FRU designated area as a circular buffer starting from offset location 0xFA to 0xFE (1 fault per each offset location). When all the byte offset locations (0xFA to 0xFE) are filled with data, the recording will resume from offset 0xFA again and continue to the next offset up to offset 0xFE. The black box

records shall remain in EEPROM or memory until being erased by user either by I2C write function or by clearing the

firmware/EEPROM.

Firmware coding	Hex	Definition Comment
	0x00	Unused, empty, no fault
#define (reserved)	0x01	Reserved (do not use)
#define PRIMARY_OTP	0x02	Primary OTP
#define SECONDARY_OTP	0x03	Secondary OTP
#define (reserved)	0x04	Reserved (do not use)
#define SCP_FAULT	0x05	Short Circuit Fault
#define OCP_FAULT_220V	0x06	OCP Fault with high line input
#define OCP_FAULT_110V	0x07	OCP fault with low line input
#define OVP_FAULT	0x08	OVP fault
#define DC12V_OVP_FAULT	0x09	12V OVP fault
#define DC12V_UVP_FAULT	0x0A	12V UVP fault
#define (reserved for AC lost)	0x0B	Reserved (do not use)
#define FAN2_FAULT	0x0C	Fan 2 Fault
#define FAN1_FAULT	0x0D	Fan 1 Fault
#define OPP_FAULT	0x0E	OPP Fault
#define OTHER_FAULT	0x0F	Other Fault

The black box function should not populate any black box data during normal operation or during normal intended power on/off (PSON on/off toggling) conditions.

13. Serial Number:

CPS-5011-4A41: 501144YWWRMSSSS

14. Mechanical Drawing: