HP201-AG

Storage Barebone
User's Manual

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Document Release History

Release Date	Version	Update Content
November, 2021	1	User's Manual release to public.
September, 2022	1.1	Section 4.11/ Section 5.2.10 Firmware SOP update.
December, 2023	1.2	Add new section: 4.12 BIOS Post Code.

Preface

Copyright

Trademarks

Changes

The material in this document is for information purposes only and is subject to change without notice.

Warning

1. A shielded-type power cord is required in order to meet FCC emission limits and also to prevent interference to the nearby radio and television reception. It is essential that only the supplied power cord be used.
2. Use only shielded cables to connect I/O devices to this equipment.
3. You are cautioned that changes or modifications not expressly approved by the party responsible for compliance could void your authority to operate the equipment.

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Instruction Symbols

Special attention should be given to the instruction symbols below.

NOTE	This symbol indicates that there is an explanatory or supplementary instruction.
CAUTION	This symbol denotes possible hardware impairment. Upmost precaution must be taken to prevent serious hardware damage.
WARNING	This symbol serves as a warning alert for potential body injury. The user may suffer possible injury from disregard or lack of attention.

Safety Instructions

Before you commence, please attentively read the following important discretions below. All cautions and warnings on the equipment or in the manuals should be circumspectly noted and reviewed.

Always ground yourself to prevent static electricity.
請全程接地，以防止靜電。
请全程接地，以防止静电。
Всегда заземляйте себя, чтобы избежать статического электричества.
Aard jezelf altijd om statische elektriciteit te voorkomen.

- Firmly ground yourself at all times when installing or assembling the internal components of the server. Most of electronic components in the server are highly sensitive to electrical static discharge.
- Use a solid grounding wrist strap and distinctively place all electronic components in static-shielded devices to prevent static. Grounding wrist straps can be purchased in any electronic supply store.
- Confirm that the power source is turned off and then disconnect the power cords from your system before performing any type of installation or manual servicing. A sudden surge of power could serverly damage the sensitive electronic components.
- Do not precipitously open the system's top cover. If you must open the cover for maintenance purposes, only a trained technician should be allowed to proceed this action. Integrated circuits on computer boards are highly sensitive to static electricity. Before operating a board or integrated circuit, touch an unpainted portion of the system unit chassis for a couple of seconds to discharge any static electricity on your body.

Place the server in a stable environment.
請將伺服器放置在穩定的環境中。
请将伺服器放置在稳定的环境中。
Поместите сервер в стабильную среду.
Plaats de server in een stabiele omgeving.

- Place this equipment on a stable surface when installing. A small mild drop or fall could cause fatal injury to both the equipment and the person handling the equipment.
- Please keep this equipment away from humidity to prevent vast rust and disintegration.
- Carefully and accurately mount the equipment into the rack. Uneven mechanical loading may lead to hazadous consequences.
- This equipment is to be installed for operation in an environment with maximum ambient temperature below 35°C.
- Review the environment before performing any installation or servicing. Keep the equipment away from hazardous and uneven grounds.
- This server must be installed only in Restricted Access Locations.

Handle equipment with care.
請謹慎操作設備。
请谨慎操作设备。
Обращайтесь с оборудованием осторожно.
Behandel de apparatuur voorzichtig.

- Do not cover the openings of the system. The openings on the system are for air convection, which intentionally protect the equipment from overheating.
- Never pour any liquid into ventilation openings of the system. This could cause catastrophic fire or electrical shock.

- Ensure that the voltage of the power source is within the specification on the label when connecting the equipment to the power outlet. The current load and output power of loads must be within the specification.
- This equipment must be firmly connected to reliable grounding before usage. Pay special attention to power supplied other than direct connections, e.g. using of power strips.
- Place the power cord out of the way of foot traffic. Do not place anything over the power cord. The power cord must be rated for the product, voltage and current marked on the product's electrical ratings label. The voltage and current rating of the cord should be greater than the voltage and current rating marked on the product.

Pay attention to hardware maintenance.
注意硬體維護。
注意硬体维护。
Обратите внимание на обслуживание оборудования.
Besteed aandacht aan hardware-onderhoud.

- If the equipment is not used for a long time, disconnect the equipment from mains to avoid being damaged by transient over-voltage.
- Module and drive bays must not be empty. They must have a dummy cover.
- Never open the equipment without professional assistance. For safety reasons, only qualified service personnel should open the equipment.
- If one of the following situations arise, the equipment should be checked and tested by service personnel:
  1. The power cord or plug is damaged.
  2. Liquid has penetrated the equipment.
  3. The equipment has been exposed to moisture.
  4. The equipment does not work well or will not work according to its user manual.
  5. The equipment has been dropped and/or damaged.
  6. The equipment has obvious signs of breakage.
  7. Please disconnect this equipment from the AC outlet before cleaning. Do not use liquid or detergent for cleaning. The use of a moisture sheet or cloth is recommended for cleaning.

CAUTION
The equipment intended for installation should be placed in Restricted Access Location.

CAUTION
There will be a risk of explosion if battery is replaced by an incorrect type. Dispose of used batteries according to the instructions. After performing any installation or servicing, make sure the enclosure is correct in position before turning on the power.

CAUTION
This unit may have more than one power supply. Disconnect all power sources before maintenance to avoid electric shock.

About This Manual

Thank you for choosing and purchasing AIC® HP201-AG Storage Server Barebone.

This user's manual is prepensely designed for professional technicians to perform dextrous hardware setup, basic system configurations, and quick software startup. This document pellucidly presents a brief overview of the product design, equipment installation, and firmware settings for our product HP201-AG. To download the latest version of this manual, please refer to the AIC® website: https://www.aicipc.com/en/productdetail/51170.

Chapter 1 Product Features

HP201-AG is a flexible 2U 4 node hyper-converged server that supports 24 hot swap 2.5-inch drives bays for NVMe SSDs(U.2)/SATA/SAS. With the maximization of the memory capacity and add-on card installation, this server is specifically designed to accommodate diverse corporations and enterprises for managing heavy workloads and multiple applications.

Chapter 2 Hardware Setup

A server is composed of multiple components and metal brackets. This chapter displays an easy installation guide for assembling the hardware in this product. The installation and removal of the internal component of the server are performed for technicians only. Utmost caution for proceeding to set up the hardware is highly advised. Most of the components are highly fragile and vulnerable to exterior influence. Do not endanger the device by placing the device in an unstable environment.

Chapter 3 Hardware Settings

System boards are placed in the server to operate the whole system.This chapter elaborates the overall layout of the system board which may vary according to the system. Multifarious connectors, jumpers, and LED functions are listed in this chapter. These descriptions assist professional technicians to configure different settings of the motherboard and confirm the placement of each connector and jumper.

Chapter 4 BIOS Configuration Settings

BIOS(Basic Input Output System) is a firmware employed to operate the server's initialization and to manage optimal runtime services for server systems. This chapter introduces the key features of BIOS, including the descriptions and option keys for diverse functions. These details provide users to effortlessly navigate and configure the input/output devices.

Chapter 5 BMC Configuration Settings

This chapter illustrates the diverse functions of IPMI BMC, including the details on logging into the web page and assorted definitions. These descriptions are helpful in configuring various functions through Web GUI without entering the BIOS setup. For more information of BMC configurations, please refer to IPMI BMC (Aspeed AST2500) User's Manual for a more detailed description.

Chapter 6 Technical Support

For more information or suggestion, please contact the nearest AIC® corporation representative in your district or visit the AIC® website: https://www.aicipc.com/en/index. It is our greatest honor to provide the best service for our customers.

Chapter 1. Product Features

HP201-AG is a high density storage server that includes motherboard, chassis, power supply, and disk drives. For more information about our product, please visit our website at https://www.aicipc.com/en/index.

Before removing the subsystem from the shipping carton, visually inspect the physical condition of the shipping carton. Exterior damage to the shipping carton may indicate that the contents of the carton are damaged. If any damage is found, do not remove the components; contact the dealer where the subsystem was purchased for further instructions. Before continuing, first unpack the subsystem and verify that the number of components in the shipping carton is accurate and in good condition.

1.1 Box Contents

This product contains the components listed below.
Please confirm the number and the condition of the components before installation.

Pre-installed into the system		Number
✓	1600W redundant power supply 80+ Platinum	1+1
✓	2.5-inch external hot swap disk drive tray (6 * NVMe/SAS/SATA per node)	24
✓	M.2 internal disk drive tray (M.2 (NGFF)/M-Key/2280/Supports SATA or PCIe x2))	2
✓	Heat sink	2
✓	Easy swap 60*56mm fan	4
✓	Easy swap 60*38mm fan	1
✓	AIC® Auriga motherboard	1
✓	24-port NVMe/SAS/SATA backplane with high-density connectors to bridge riser board	1
Accessory Item		**Number**
✓	Screw for 10 * 2.5" HDD, bottom: F(+),M3*4L,NI	96
✓	Screw for 24 * 2.5" HDD, bottom: F(+),M3*4L,NI	40
✓	EPE foam for front board: 563*510*105H	1
✓	EPE foam for rear board: 563*510*105H	1
✓	EPE foam for front tray: 563*300*145H	1
✓	EPE foam for rear tray: 563*300*145H	1
✓	EPE pad for rail: 130*100*45T	2
✓	Power cord	vary per region
BTO	28-inch tool-less slide rail assembly	1
	2.5-inch internal hot swap SATA disk drive tray (2 per node)	8
	2000W redundant power supply 80+ Platinum	1+1

Product features are subject to change without notice.

1.2 Specifications

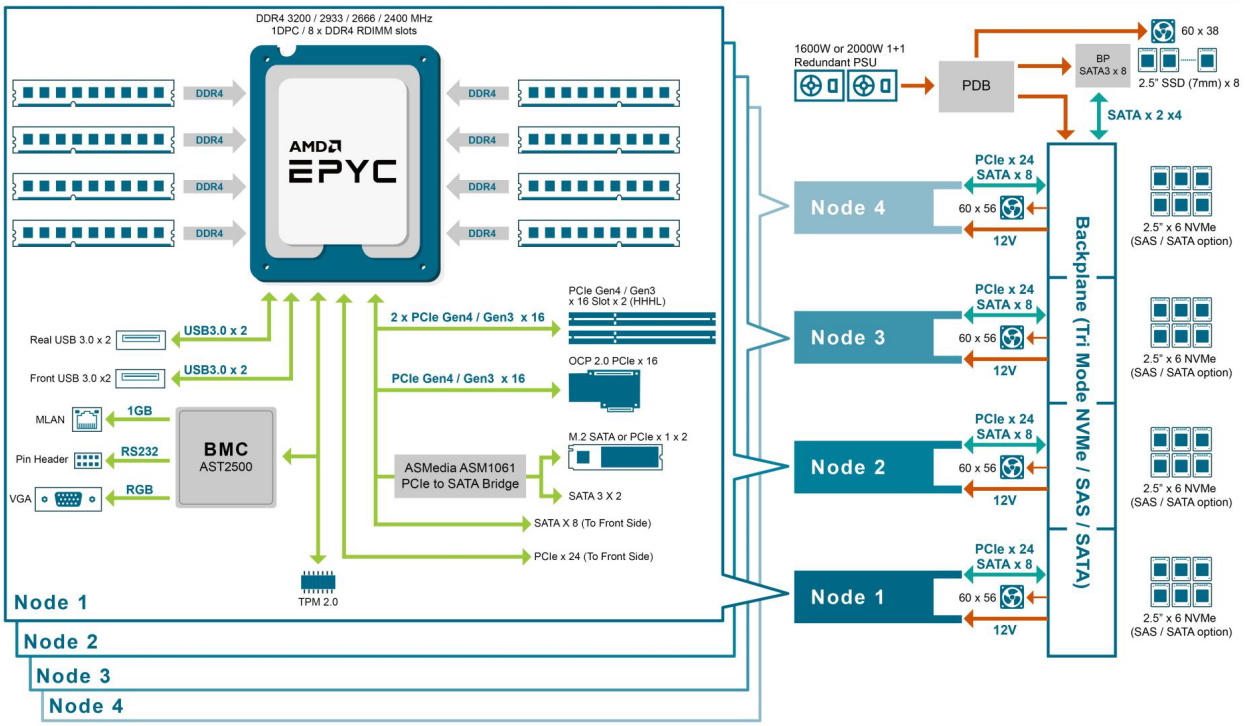
Dimensions (W x D x H)	mm : 438 x 780 x 87.5		
	inches : 17.2 x 30.7 x 3.5		
Motherboard (per node)	AIC Server Board Auriga		
Processor (per node)	Processor Support	• Single AMD EPYC™ 7003/7002/7001 processor • Supports CPU TDP up to 280W (support by EPYC™ 7003 CPU) **Please contact AIC Technical Support for more info/details about optimized CPUs and specialized system.*	
	Socket Type	SP3	
Chipset Support (per node)	AMD EPYC™ SOC		
System Memory (per node)	• DDR4 3200/2933MHz RDIMM/LRDIMM • Total 8 memory slots ; 8 channels • Supports up to 2TB (support by EPYC™ 7003/7002 CPU) • Supports NVDIMM feature		
Front Panel	Node power on/off		
LEDs	• Node power status • Node ID • BMC alert		
Drive Bays	External	2.5" hot swap	24 (6 x NVMe/SAS/SATA per node)
	Internal	2.5" hot swap	8 (2 x SATA per node) (Option)
		M.2	2 x M.2(NGFF) / M-Key / 2280 / Supports SATA or PCIe x2
Backplane	1 x 24-port NVMe/SAS/SATA backplane with high-density connectors to bridge riser board		
Expansion Slots (per node)	PCIe 3.0/4.0	• 2 x16 slots (LP) • 1 x16 OCP Mezzanine V2.0 **Please contact AIC Technical Support for more info/details about OCP card.*	
Rear I/O (per node)	LAN	1 x RJ45 dedicated to BMC management	
	USB	2 x USB 3.0	
	VGA	1 x external DB-15 VGA port	
	Others	• Power on/off • System ID • BMC alert LED	
TPM Support	2.0 onboard		
Power Supply	1600W 1+1 redundant power supply 80+ Platinum • AC INPUT : 200~240V,50/60Hz,12A (except China/Taiwan) • AC INPUT : 200~240V,50/60Hz,10A (for China/Taiwan) 2000W 1+1 redundant power supply 80+ Platinum (BTO) • AC INPUT : 200~240V,50/60Hz,15A • Socket type: C20 (Power cord type: C19)		
System Cooling	• 4 x 60x56mm easy swap fans • 1 x 60x38mm easy swap fan		

Riser Card (included) (per node)	RC-PE1U02-Z2	1 x16 PCIe slot
	RC-PE1U18-TY	1 x16 PCIe slot
System BIOS	BIOS Type	Insyde UEFI BIOS
	BIOS Features	• ACPI • PXE • IPMI KCS interface • SMBIOS • SRIOV • iSCSI • TPM • PCIe Hotplug
On-board Devices	SATA/NVMe	• 2 x SATA 6.0 Gb/s • 2 x SATA 6.0 Gb/s by M.2 (M-key) supports up to 22110 (can be confirgured as 2 x PCIe x1 M.2)
	BMC	Aspeed AST2500 Advanced PCIe Graphics & Remote Management Processor • Baseboard Management Controller • Intelligent Platform Interface 2.0 (IPMI 2.0) • iKVM, Media Redirection, IPMI over LAN, Serial over LAN • HTML5 • Redfish • SMASH Support
	Graphics	Aspeed AST2500 Advanced PCIe Graphics & Remote Management Processor • PCIe VGA/2D Controller • 1920x1200@60Hz 32bpp
System Management	• Baseboard Management Controller • Intelligent Platform Interface 2.0 (IPMI 2.0) • iKVM, Media Redirection, IPMI over LAN, Serial over LAN • SMASH Support	
Environmental Specifications	• Storage temperature : -10ºC(14ºF) ~ 60ºC(140ºF) • Operating temperature : 0ºC(32ºF) ~ 35ºC(95ºF) • Storage operating humidity : 5%~95% non-condensing	
Gross Weight	(w/ PSU & Rail)	kgs : 36 lbs : 79.4
Packaging Dimensions	(W x D x H)	mm : 605 x 1100 x 320 inches : 23.6 x 42.9 x 12.5
Mounting	Standard	28" tool-less slide rail

CAUTION

Please be noted that if the product that you purchase supports 2000W 1+1 redundant power supply unit, you will require C19 power cord for a higher rated current (15A) support.

1.3 System Block Diagram



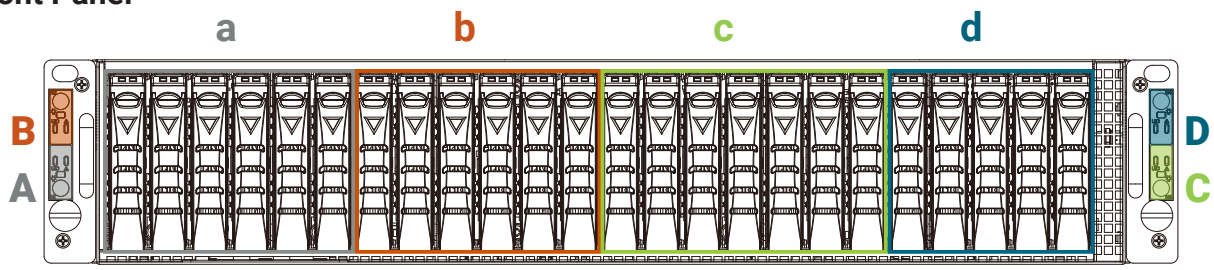
1.4 Feature

HP201-AG is a reliable 2U 4 node hybrid storage server barebone with 24 * 2.5-inch hot-swap drives bays. This product is designed to accommodate the AIC® patented server-board, Auriga, which supports one AMD EPYC™ 7000-series processor and 8 DDR4 2400/2666 DIMM to offer greater performance, efficiency, and utility for our customers. Featuring the AMD EPYC™ 7000-series processor as the core design of the serverboard, which is emphasized for its outstanding performance, great memory bandwidth, and high security based on “Zen” microarchitecture, this product enhances these advantages by upgrading its system expansion.

In addition to integrating more memory capacity and system expansion to the server board, Auriga offers immediate and efficient management with Onboard Baseboard Management Controller and greater I/O extension. Featuring IPMI 2.0 and Aspeed AST2500 Advanced PCIe Graphics, the server board offers support for iKVM, Media Redirection, IPMI over LAN, Serial over LAN, HTML5, and Redfish.

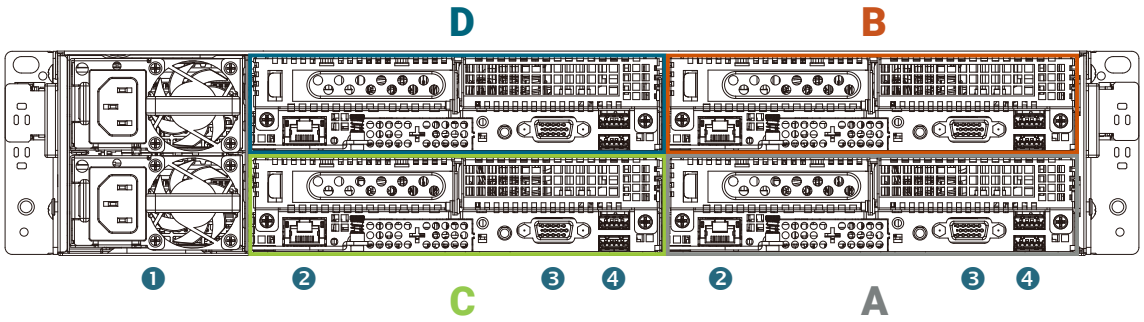
- 2U 4-Node hybrid storage server supports 24 hot swap 2.5” drive bays for NVMe SSDs (U.2)/SAS/SATA
- Supports AMD EPYC™ 7002/7001 processor
- Maximizing the use of the numbers of memory, add-on cards, and drives in one single system
- Onboard Baseboard Management Controller for system management and IPMI control
- 3 * PCIe x16 extensions on each node
- Front-to-back airflow and easy swap redundant fans to provide optimal thermal conditions
- Customizable to meet your requirements

Front Panel



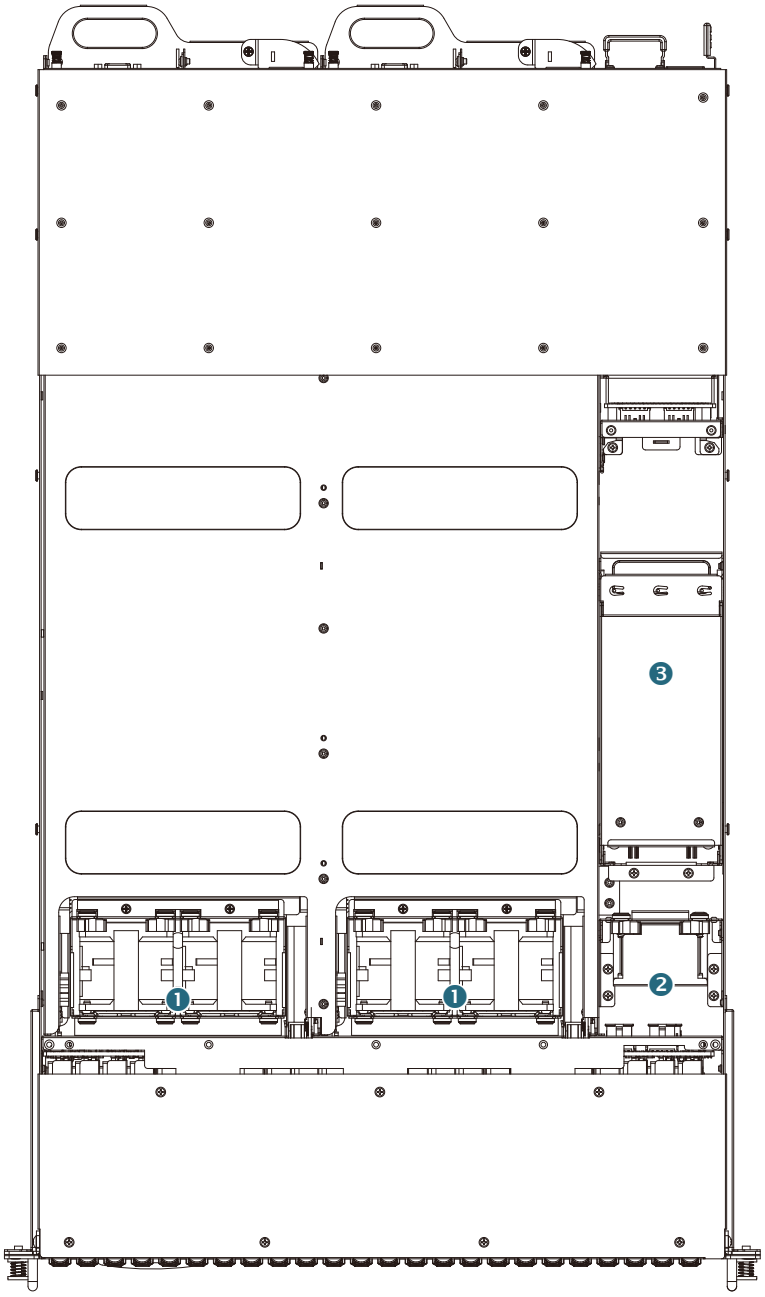
Item	Description	Item	Description
⏻	Node Power Button	ID	Node ID LED
💡	Node Power Status LED	⚠	BMC Alert LED
A~D	Node Control Panel	a~d	Corresponding Control Drive

Rear Panel

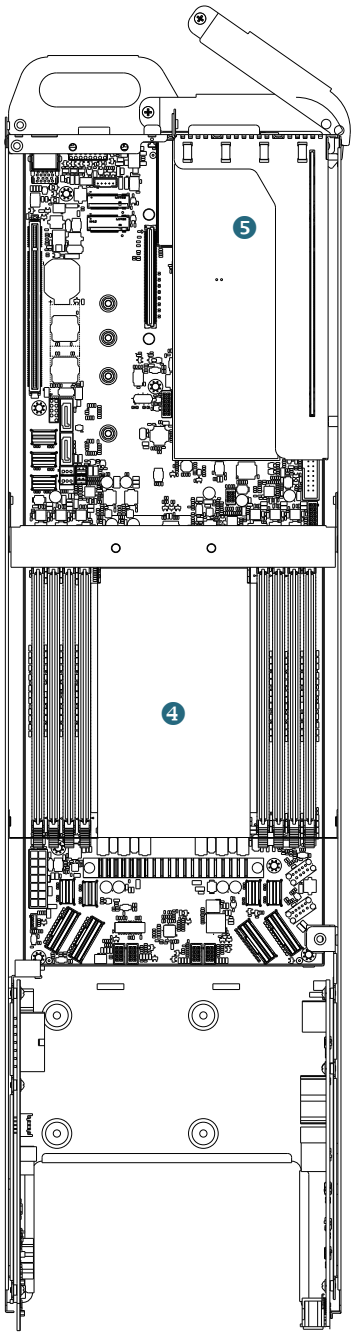


Item	Content	Description
1	PSU socket	1600W 1+1 redundant power supply 80+ Platinum • AC INPUT : 200~240V,50/60Hz,12A (except China/Taiwan) • AC INPUT : 200~240V,50/60Hz,10A (for China/Taiwan) 2000W 1+1 redundant power supply 80+ Platinum (BTO) • AC INPUT : 200~240V,50/60Hz,15A • Socket type: C20 (Power cord type: C19)
2	LAN port	1 * GbE RJ45 dedicated to BMC management
3	VGA port	1 * external DB-15 VGA port
4	USB port	2 * USB 3.0 Type A
A~B	Node Placement	

Top View



Node Top View



Item	Content	Description
1	Fan	4 * 60x56mm easy swap fans
2	Fan	1 * 60x38m easy swap fan
3	Disk Drive	8 * 2.5-inch disk drive (optional)
4	Server board	AIC® Auriga
5	Riser Card	1 * PCIex16

Chapter 2. Hardware Setup

This section describes a simple instruction guide for installing the hardware components on the serverboard system. Turn off and unplug all system and peripheral devices before proceeding.

2.1 Central Processing Unit

The serverboard supports a single AMD EPYC™ 7000-series and socket type SP3.

2.1.1 Processor Installation

To ensure a safe and easy setup, you need to prepare before installation:

☑ a T20 Torx screwdriver

☑ ESD wrist strap/mat and conductive foam pad

CAUTION
The pins of the processor socket are vulnerable and easily susceptible to damage if fingers or any foreign objects are pressed against them. Please keep the socket protective cover on when the processor is not installed.

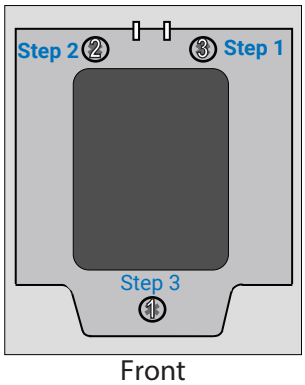
CAUTION
When unpacking a processor, hold the processor only by its edges to avoid touching the contacts.

Procedure:

① Remove the screw in the order designated in blue (the screw labeled 3⇨2⇨1) as demonstrated in figure 1. After the screws are dislodged, the load plate will automatically be ejected as demonstrated in figure 2.

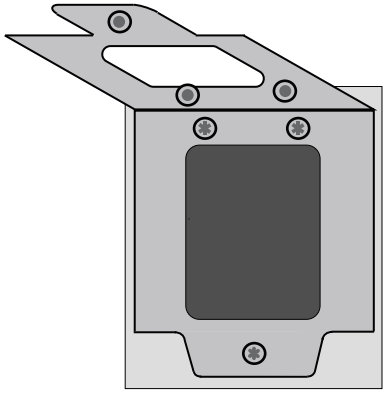
NOTE
The screws cannot be completely removed from the CPU cover.

Dislodge screw



Front

Remove top cover

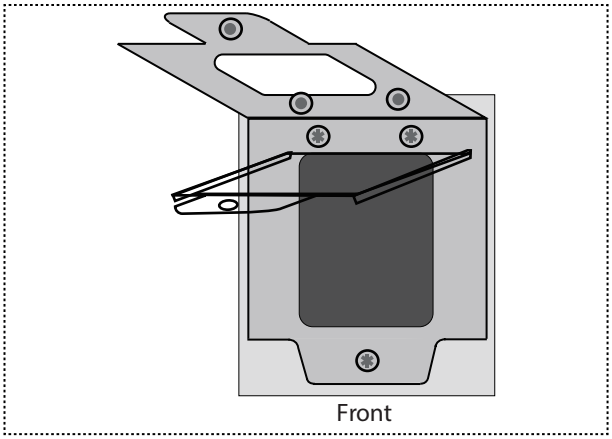


Front

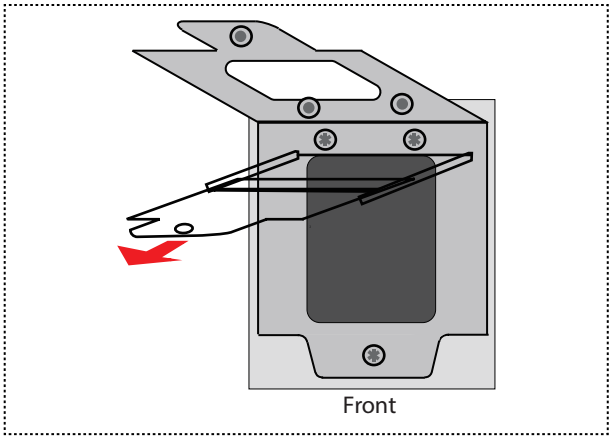
This information is provided for professional technicians only.

② Lift the carrier frame by the blue metal tab and remove the protective cover as demonstrated in figure 3 and figure 4.

Lift carrier frame

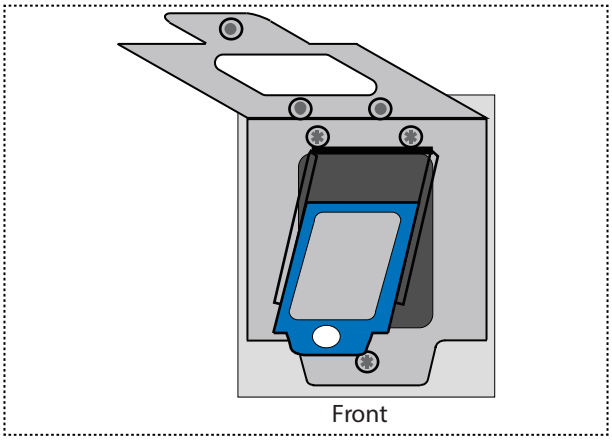


Remove protective cover



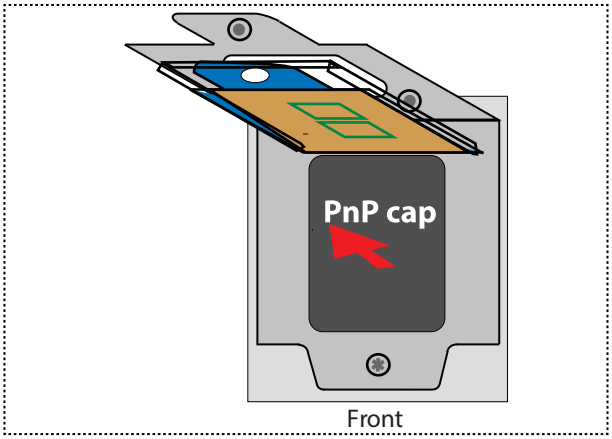
③ Insert the CPU package into the carrier frame as demonstrated in figure 5.

Insert package



④ Remove the Pick and Place(PnP) cap by lifting the it upward as demonstrated in figure 6.

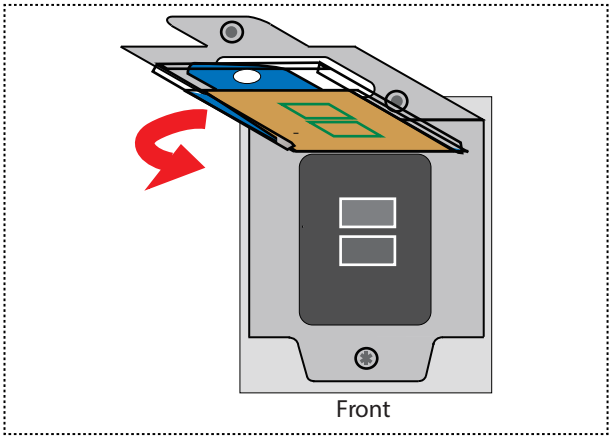
Lift PnP cap



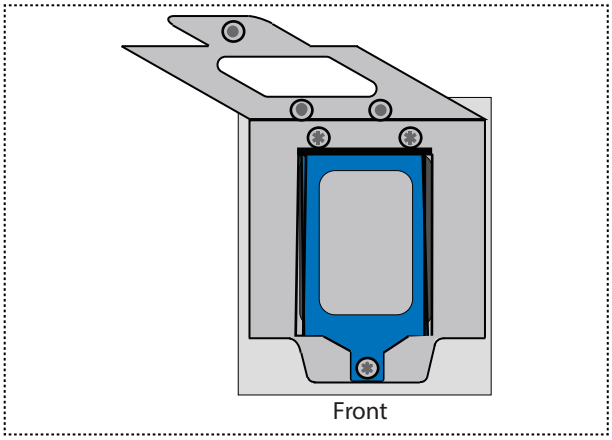
This information is provided for professional technicians only.

⑤ Close the carrier frame with the CPU package as demonstrated in figure 7. Check if the frame is properly installed as demonstrated in figure 8.

Close carrier frame

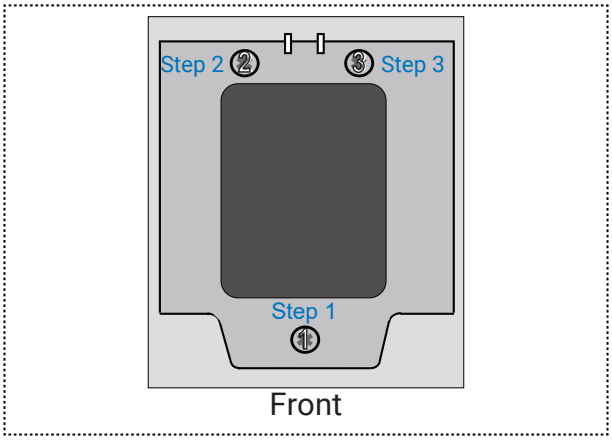


Verify installation



⑥ Close the load plate and fasten the screws in the order 1⇨2⇨3 to complete installation as demonstrated in figure 9.

Close load plate



⑦ Apply thermal grease/paste on top of the CPU assembly.

⑧ Secure the heatsink on top of the processor assembly to complete installation.

This information is provided for professional technicians only.

2.2 System Memory

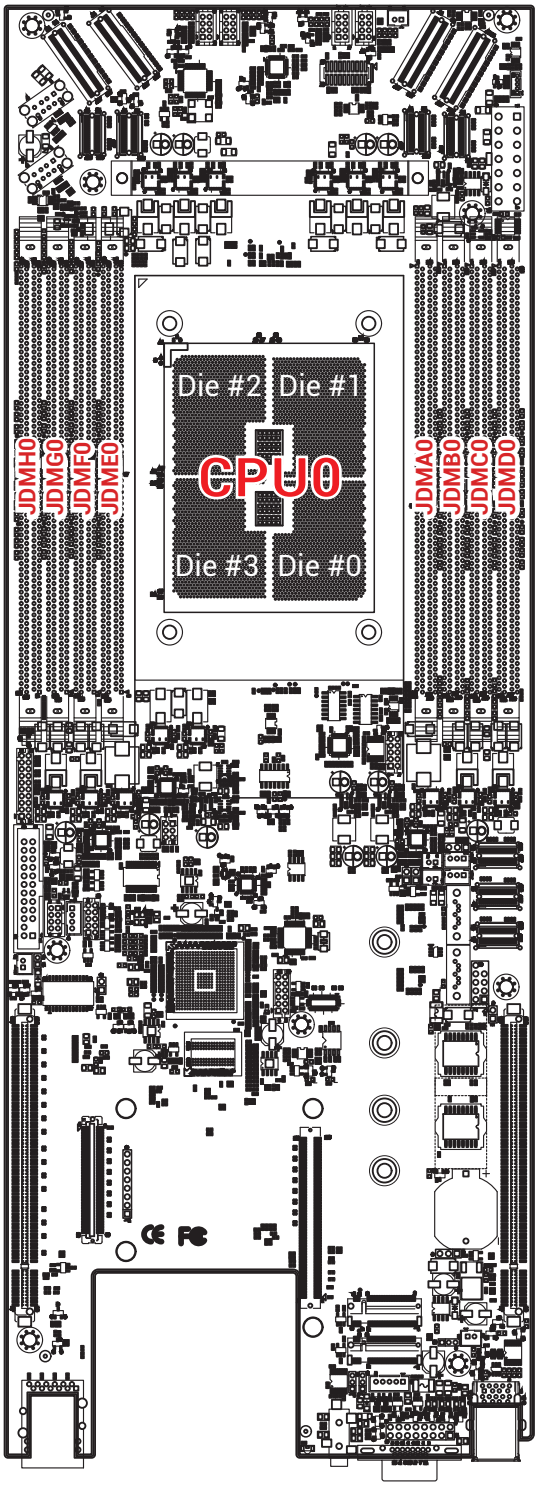
2.2.1 DIMM Placement

The DIMMs are displayed on the Auriga board as JDMA0, JDMB0, JDMC0, JDMD0, JDME0, JDMF0, JDMG0, and JDMH0 as demonstrated. JDMA0 and JDME0 are the located nearest to the CPU.

To ensure satisfactory performance, you need to:

☑ Verify the DIMM type:
This product supports DDR4 RDIMM/ LRDIMM/NVDIMM-N
with EEC(Error Correction Code).

☑ Verify if all of the DIMMs installed are of the same DIMM type to avoid memory failure and loss of performance speed.



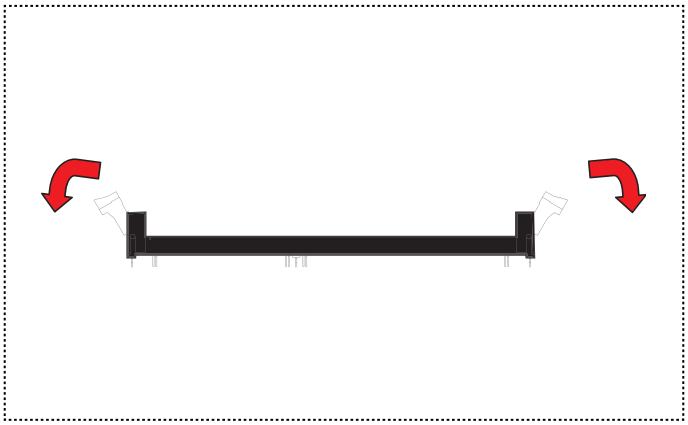
2.2.2 DIMM Population

Populate the DIMM slots according to the corresponding Die as suggested to ensure a stable system performance.

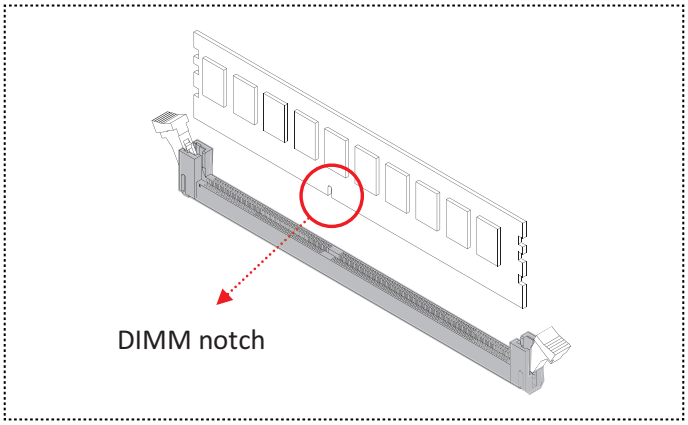
Die #0: JDMC0 / JDMD0
Die #1: JDMA0 / JDMB0
Die #2: JDMG0 / JDMH0
Die #3: JDME0 / JDMF0

2.2.3 Installation

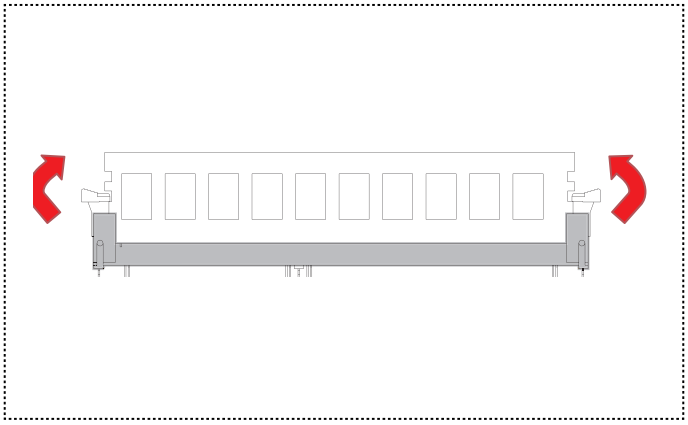
① Unlock the DIMM socket by pressing the retaining clips outward.



② Insert the memory module into the slot. Make sure that the DIMM notch is accurately positioned.



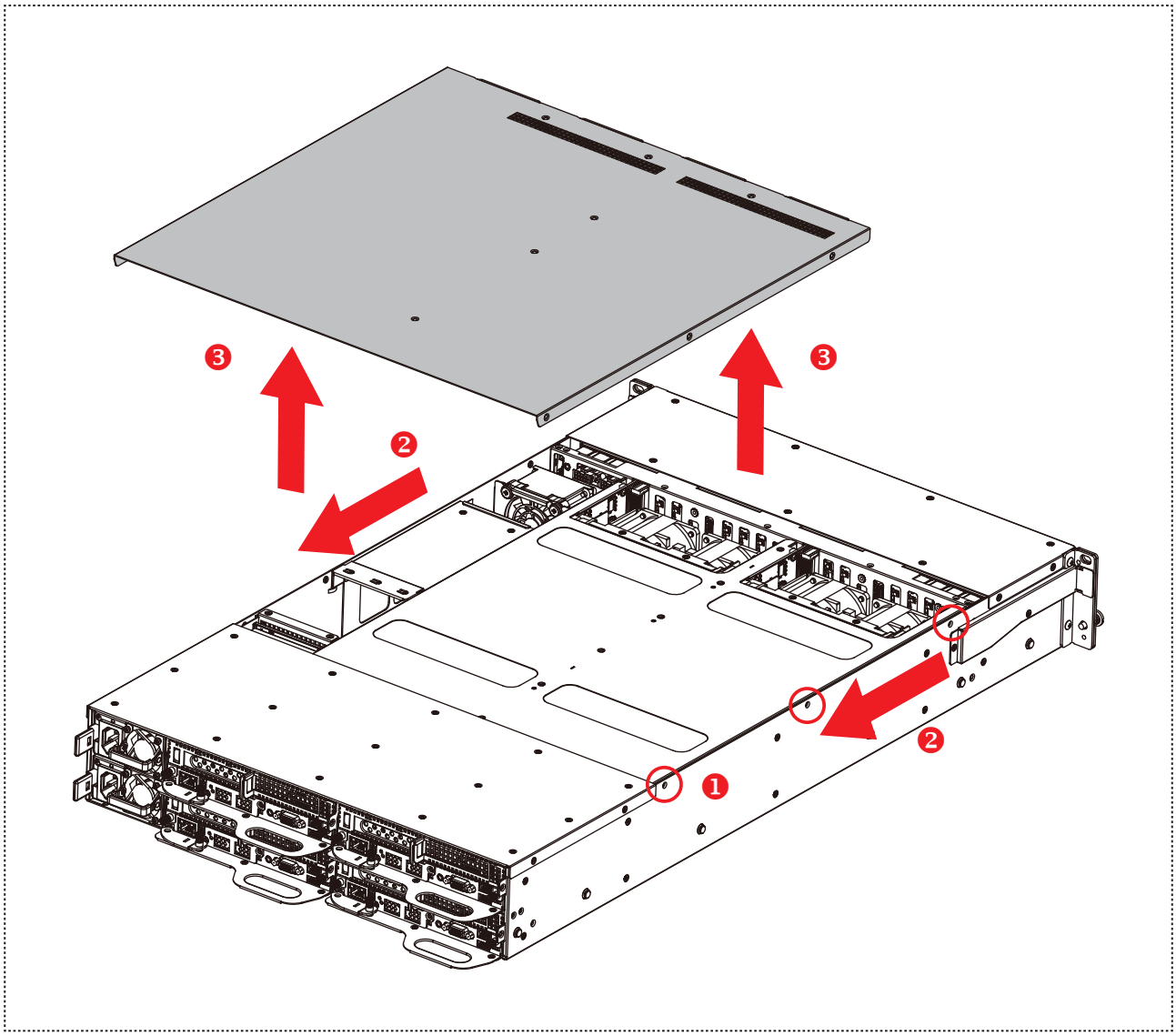
③ Close the retaining clips to complete installation.



This information is provided for professional technicians only.

2.3 Top Cover

① Dislodge the screws the secure the top cover.
② Push the cover toward the rear panel.
③ Lift the top cover upward to remove.

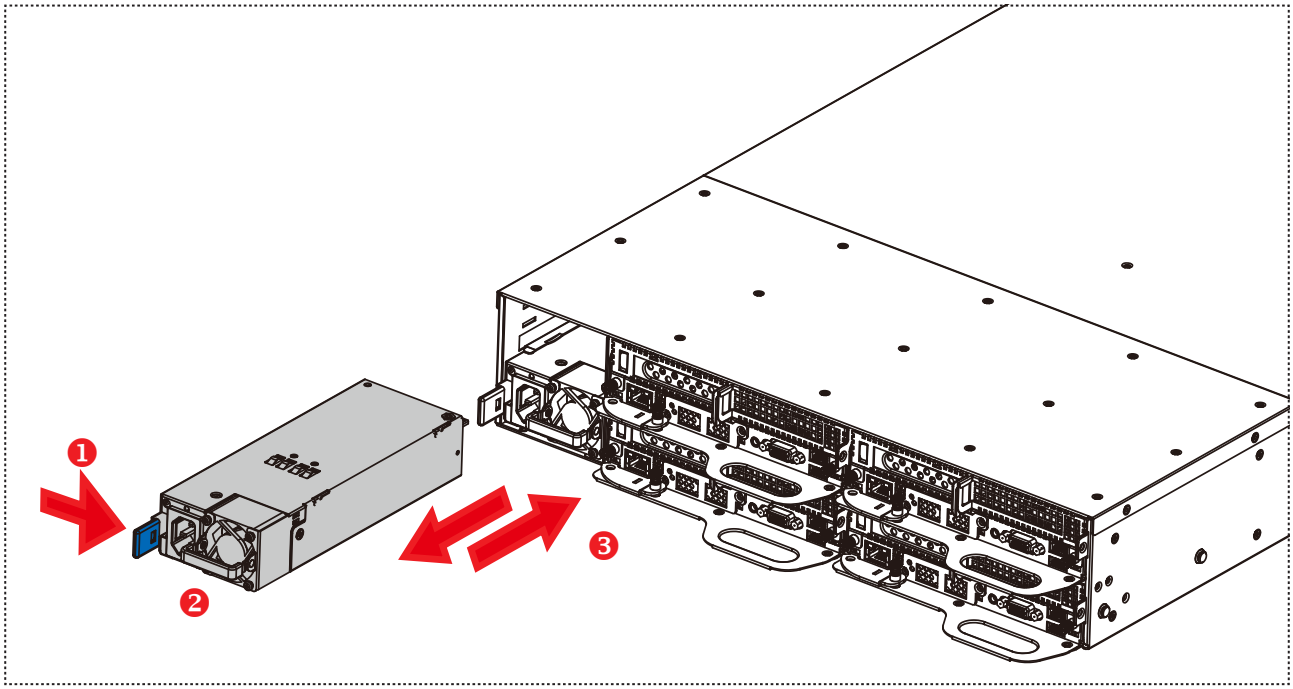


This information is provided for professional technicians only.

2.4 Power Supply Unit

2.4.1 Installation

① Press the ejector to release the module.
② Pull the handle to remove the module out of the chassis.
③ Push the replaced power supply unit into the chassis. Ensure that the module is hooked into the cage.



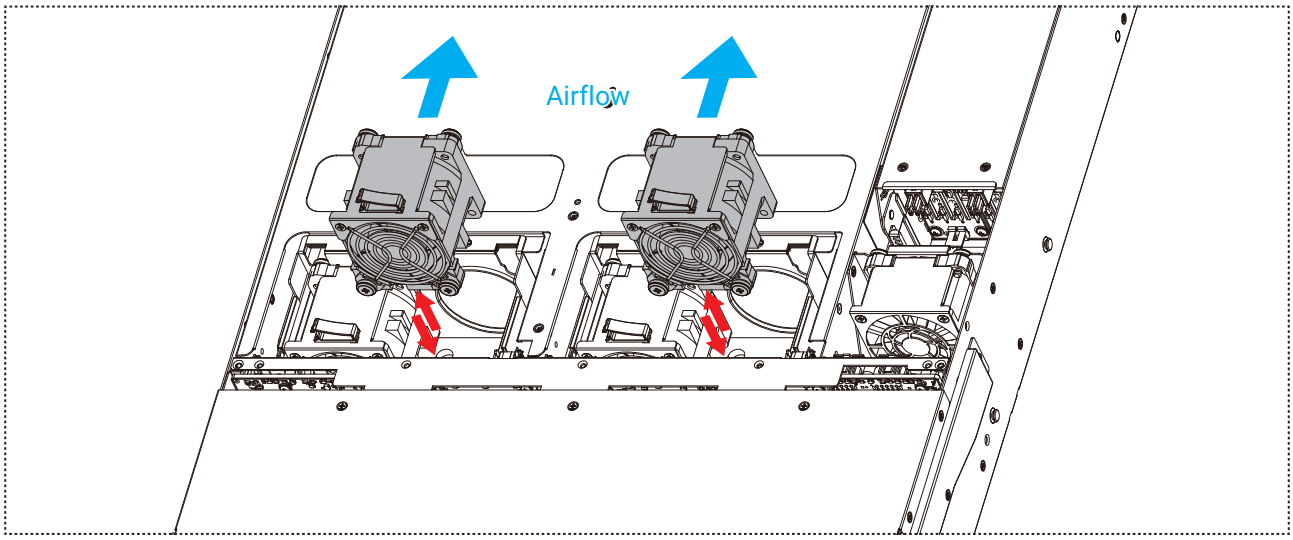
2.4.2 LED Indicator

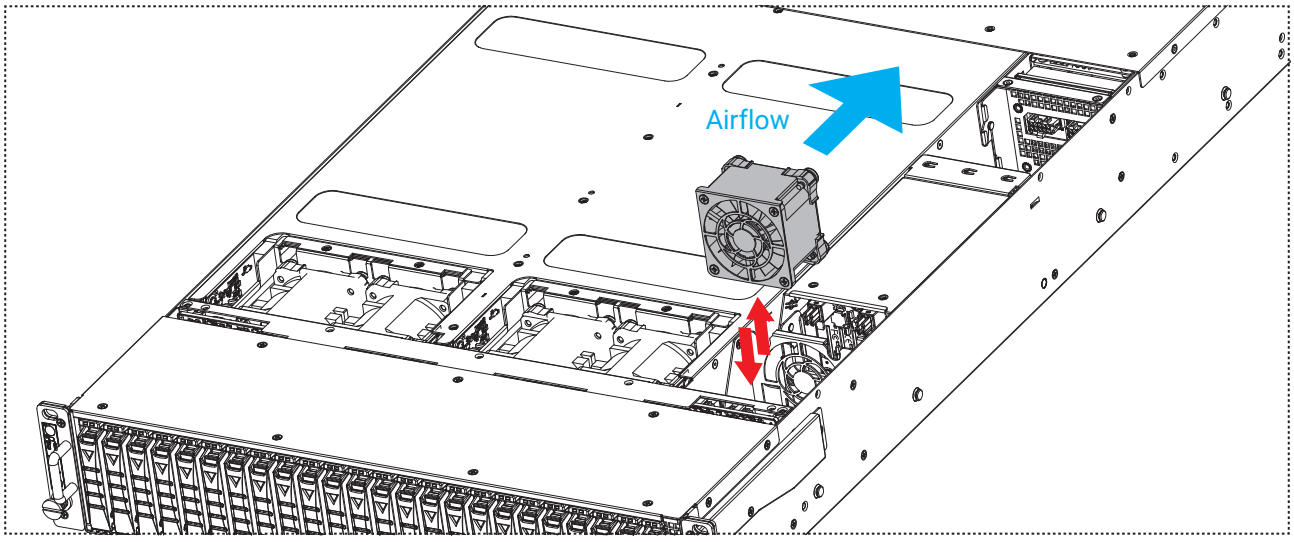
Indicator Color	Behavior
Green	Output on and Ok.
Green (blinking, 1Hz)	Only 12Vsb (PS off) or PSU is in cold redundant state.
Amber	Power supply critical event causing a shutdown; AC cord unplugged or AC power lost, failure, OCP, OVP, fan fail.
Amber (blinking, 1Hz)	Power supply warning events where the power supply continues to operate high temp, high power, high current, slot fan.

This information is provided for professional technicians only.

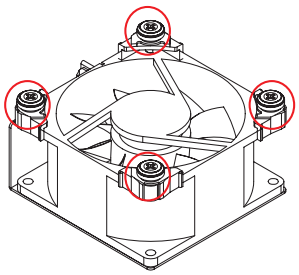
2.5 Fan

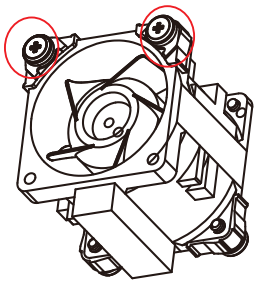
① Remove the top cover from the chassis. Please refer to Section 2.3 Top Cover.
② Unplug the cables and connectors from the server board.
③ Pull the fan out of the chassis.
④ Insert the replaced fan into the chassis. Verify the alignment of the rubber connectors of the fan and the bracket. Ensure that the fan is inserted into the correct slot.





Rubber connector



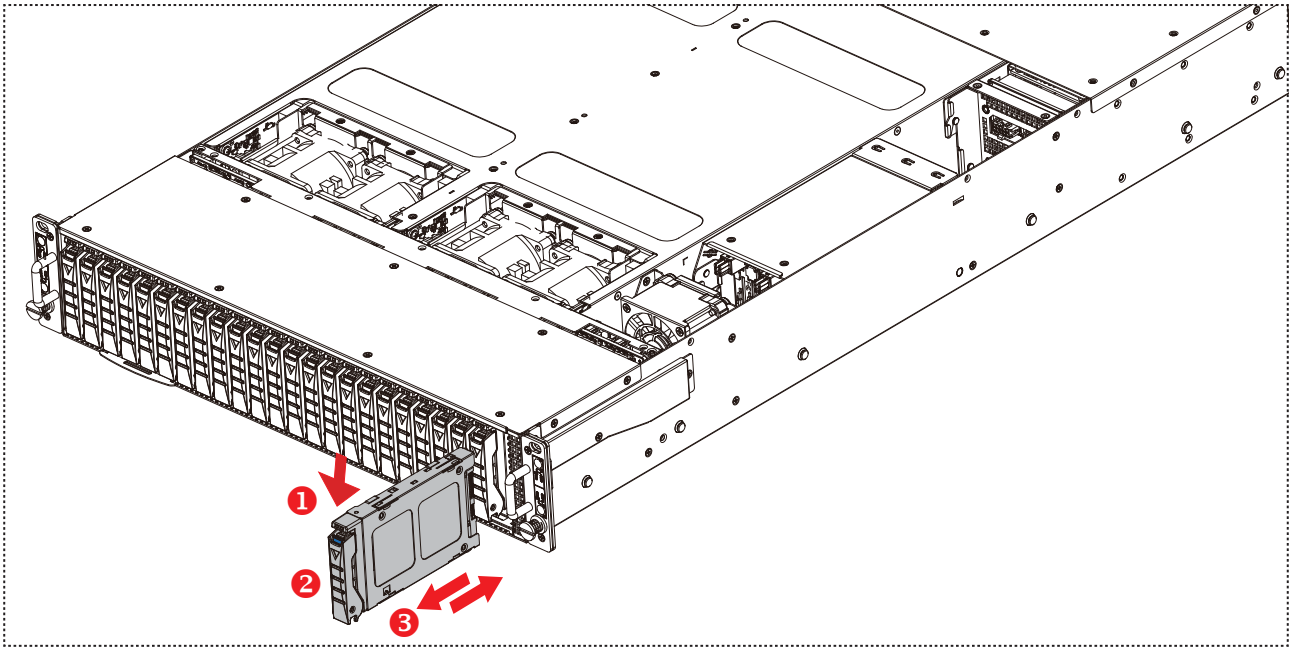


This information is provided for professional technicians only.

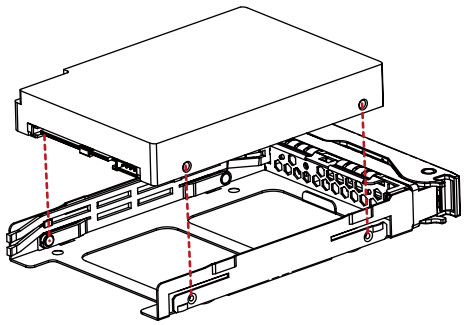
2.6 Disk Drive

2.6.1 External Disk Drive

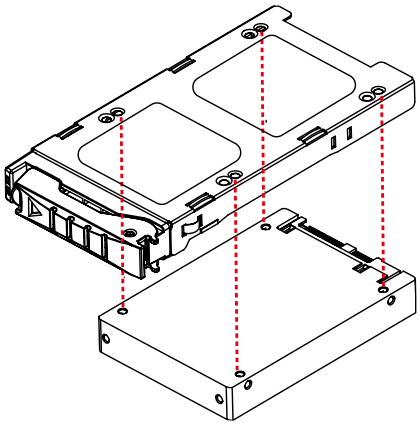
① Press the ejector on the tray to release the handle.
② Pull the tray handle completely outward.
③ Pull the drive tray out of the chassis.



④ Insert the disk drive into the tray. Ensure that the dimples on the tray match the disk drive. For additional assurance, fasten the screws * 4 on the tray to secure the disk drive.



2.5" SSD dimple placement



2.5" SSD screw placement

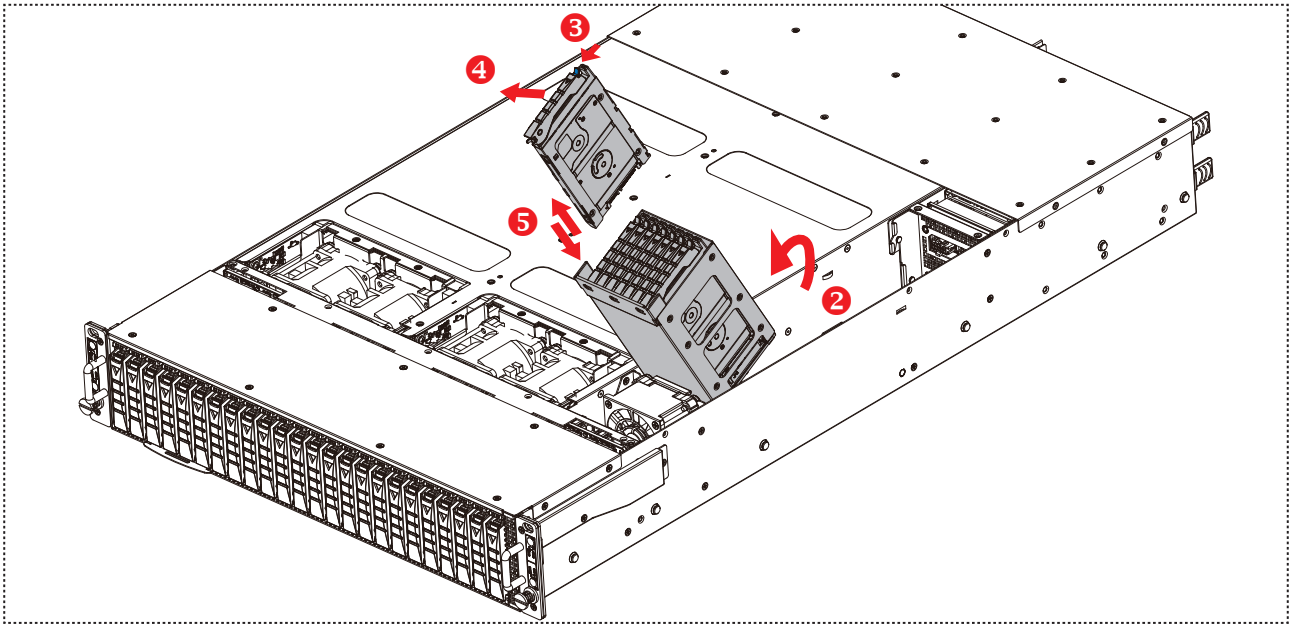
⑤ Push the tray with the installed disk drive into the end of the drive slot in the chassis.
⑥ Close the tray handle.

NOTE
For this server product, 2.5-inch disk drive trays support SSDs only. Do not use insert HDD into 2.5-inch drive tray.

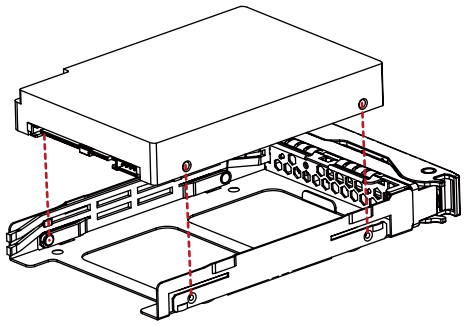
This information is provided for professional technicians only.

2.6.2 Internal Disk Drive

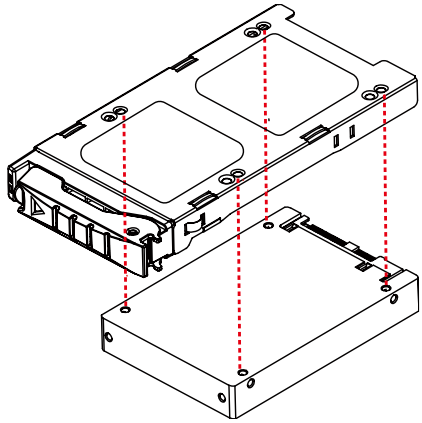
① Remove the top cover from the chassis. Please refer to Section 2.3 Top Cover.
② Lift and slightly rotate the 2.5-inch drive cage out of the chassis.
③ Press the ejector on the drive tray to release the handle.
④ Pull the drive tray outward completely.
⑤ Pull the tray out of the chassis.



⑥ Insert the disk drive into the tray. Ensure that the dimples * 4 on the tray match the disk drive. For additional assurance, fasten the screws * 4 on the tray to secure the disk drive.



2.5" SSD dimple placement



2.5" SSD screw placement

⑦ Push the tray with the installed disk drive into the end of the drive slot in the chassis.
⑧ Close the tray handle.

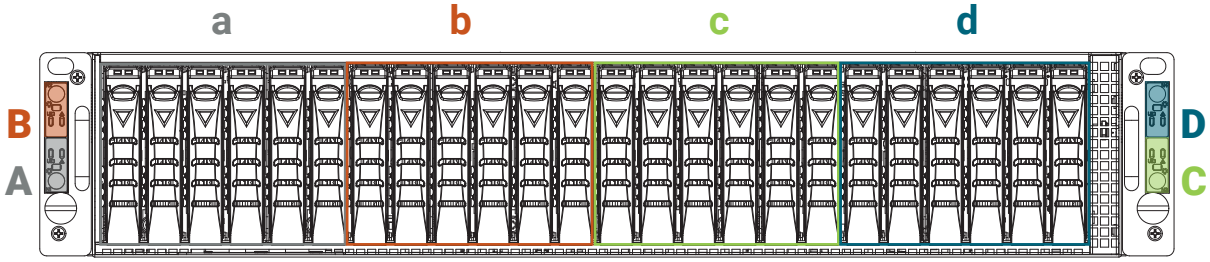
NOTE
For this server product, 2.5-inch disk drive trays support SSDs only. Do not use insert HDD into 2.5-inch drive tray.

This information is provided for professional technicians only.

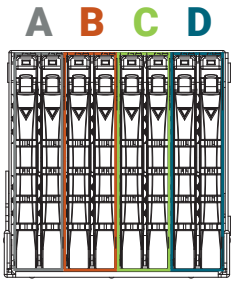
2.6.3 LED Indicator

Indicator	Behavior	Description
Blue	Solid	NVMe/SATA/SAS drive is in idle state.
	Blinking (4Hz)	NVMe/SATA/SAS is active.
	Off	NVMe/SATA/SAS is not detected or the system power is off.
Green	Blinking (4Hz)	NVMe/SATA/SAS is in locate status.
Yellow	Solid	There is a drive fault.
	Blinking (1Hz)	There is a drive rebuild. Because of legacy and cross-compatibility with SGPIO initiators, both interpretations of Rebuild should be supported.
	2 Fast Blink at 4Hz & Pause for 0.5 sec.	Predicted Failure Analysis. The drive in this slot is still working but predicted to fail soon.

2.6.4 Drive Slot Map



2.5-inch Drive Slot Map																							
1	2	3	4	5	6	1	2	3	4	5	6	1	2	3	4	5	6	1	2	3	4	5	6

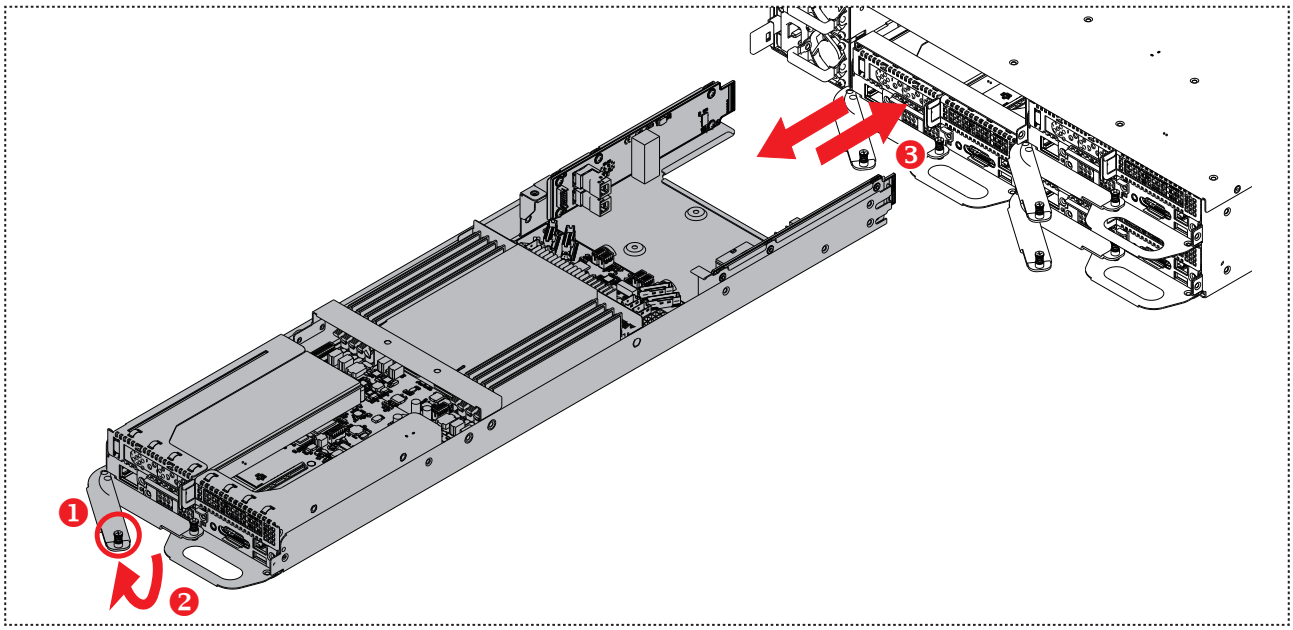


OS Drive Slot Map							
1	2	1	2	1	2	1	2

The capital letters A, B, C, D corresponds to the motherboard. Please refer to the rear panel image in Section 1.4 Feature.

2.7 Node

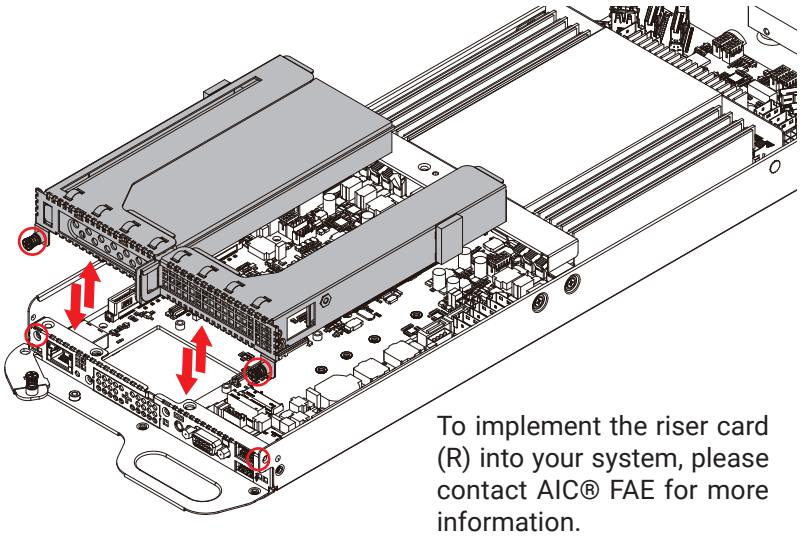
① Unscrew the captive screw to release the handle.
② Pull the handle to remove the node out of the chassis.
③ Push the replaced node into the chassis. Ensure that the tray is completed installed in the chassis.
④ Close the handle and secure the captive screw.



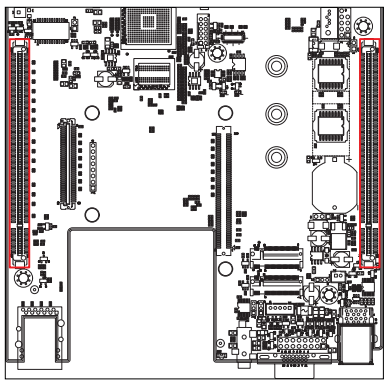
2.8 Riser Card

① Remove the node from the chassis. Please refer to Section 2.7 Node.
② Dislodge the captive screws on the cage to remove the bracket securing the riser card.
③ Pull the riser card bracket outward and upward to remove.
④ Replace the riser card.

Standard riser card (L: left-side) & BTO riser card (R: right-side)



To implement the riser card (R) into your system, please contact AIC® FAE for more information.

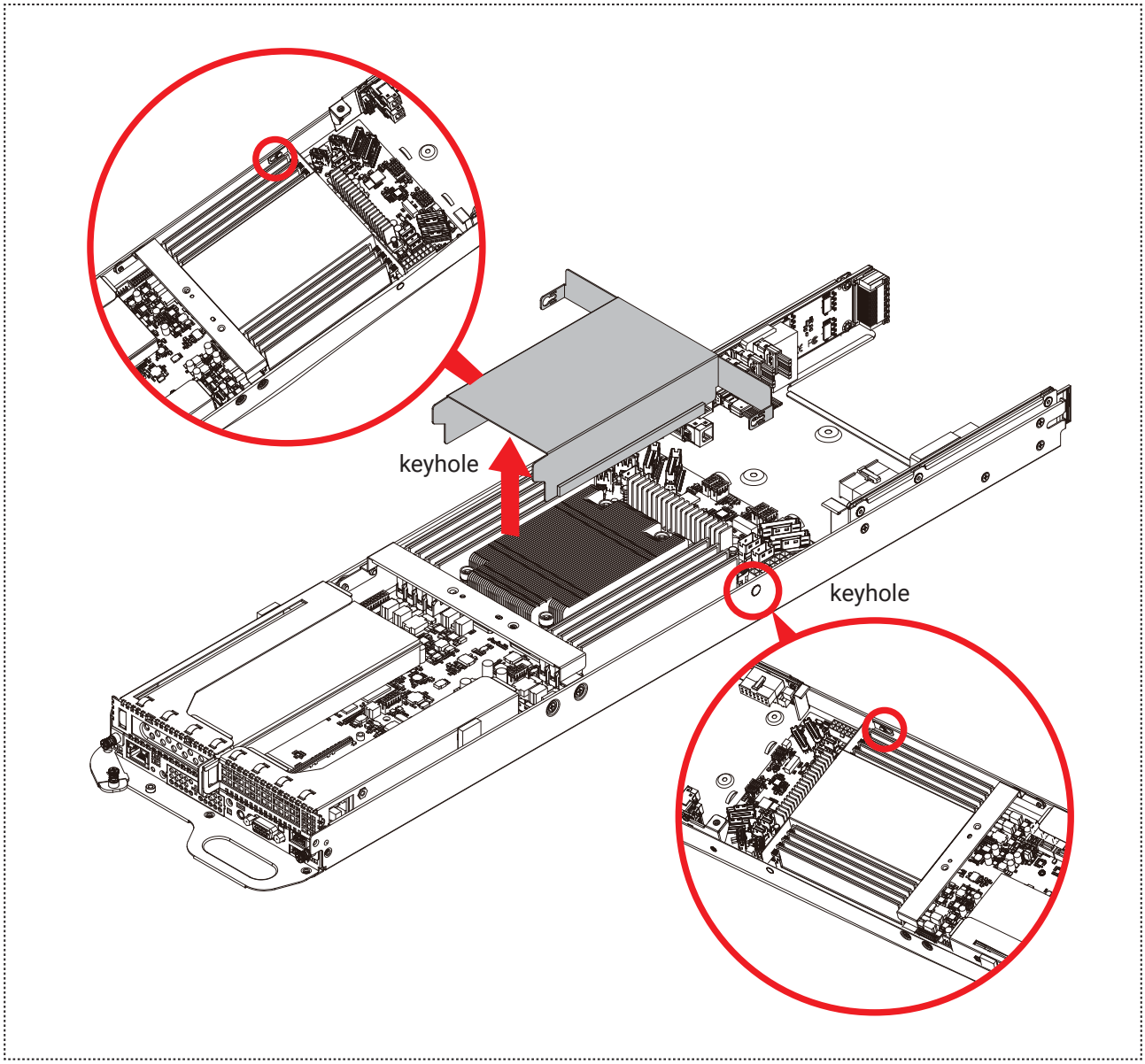


PCIe placement (top view)

This information is provided for professional technicians only.

2.9 Air Duct

① Pull the node from the chassis. Please refer to Section 2.7 Node.
② Unlock the keyholes that secure the air duct on both sides.
③ Lift the air duct update to remove.



CAUTION
Please check the placement of the air duct in the manual before installation to prevent damage to the system.

This information is provided for professional technicians only.

2.10 Slide Rail

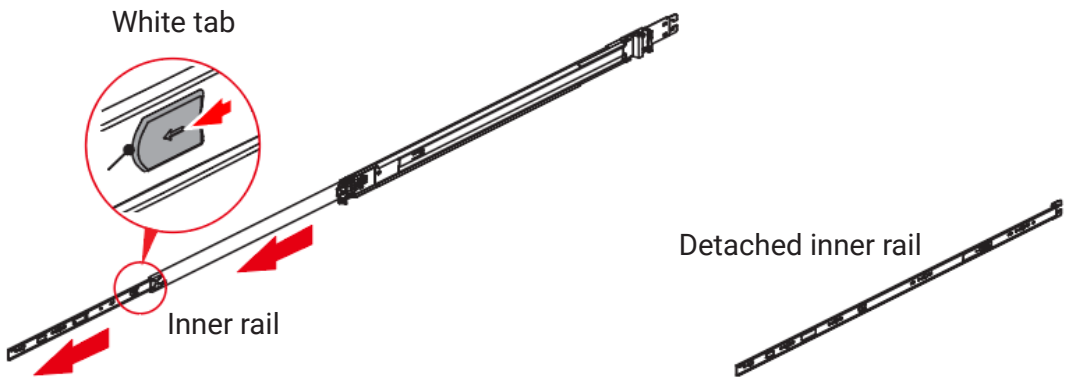
NOTE

This sections provides a basic instruction for mounting the slide rail onto the system. Tool-less rails vary per order. The rail in this manual may not exactly match the rail for your system. Please refer to the specifications or quick installation guide that came with your purchased product.

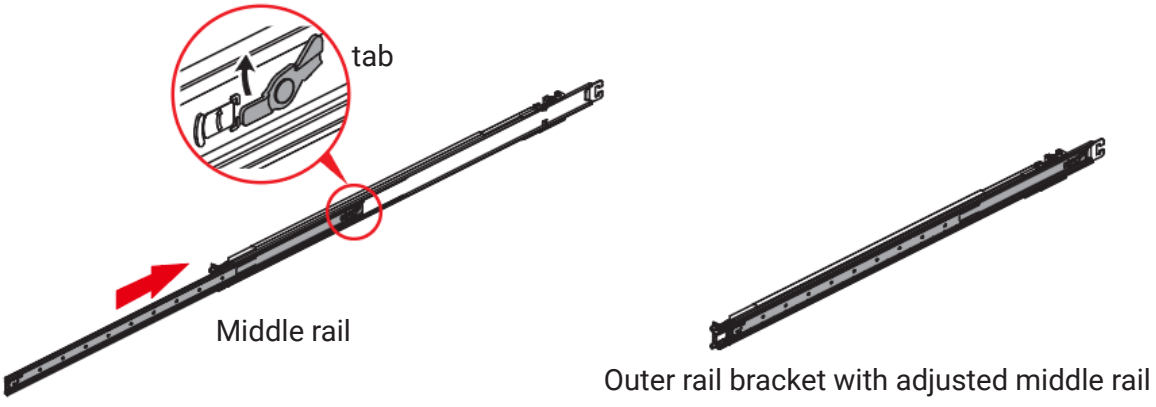
CAUTION

They rack may tilt and fall due to incorrect installation or placed on uneven grounds. The rack must be placed in a flat surface before you begin to slide the system barebone in for servicing.

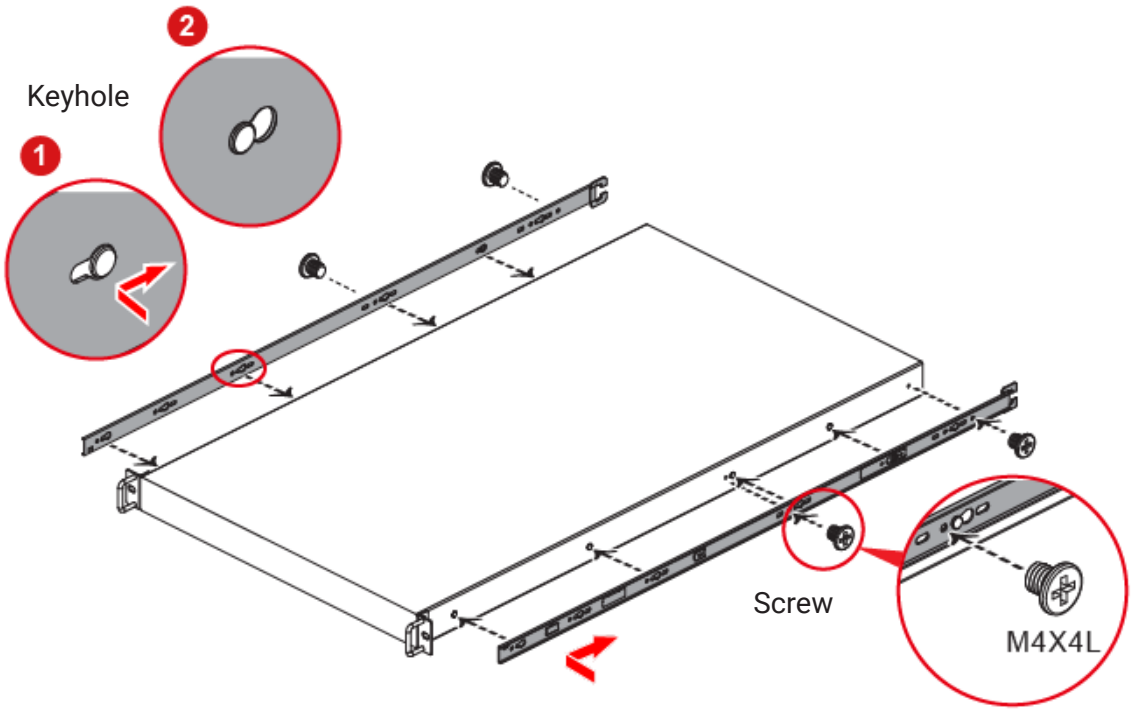
1. Pull the inner rail out of the slide rail until it clicks.
2. Detach the inner rail completely from the slide rail by pulling the white tab forward.



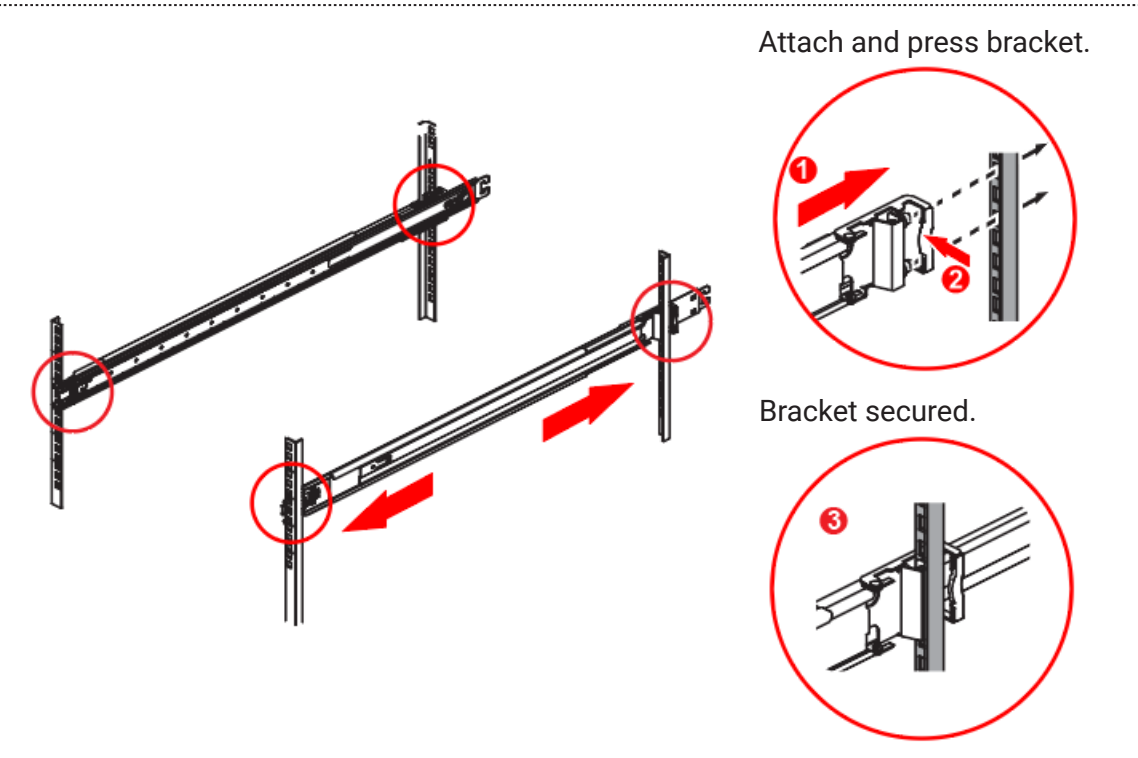
3. After the inner rail is dislodged, adjust the middle rail back to its original position by pushing the tab on the middle rail.



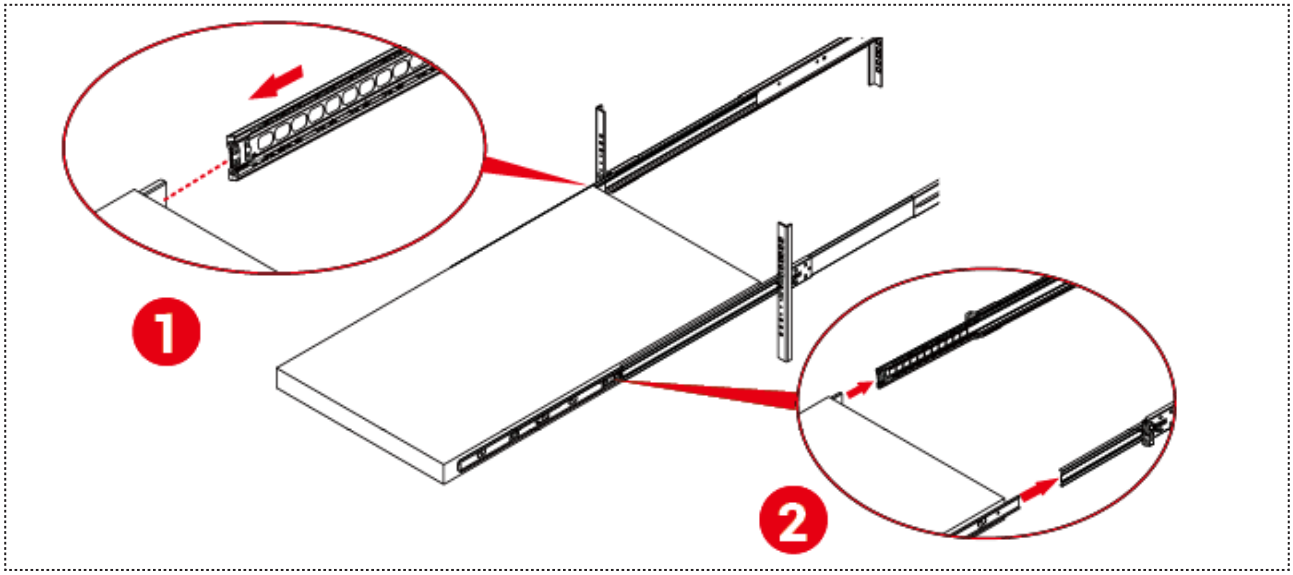
4. Install the inner rail onto the system barebone. Lock the keyholes and secure the system with M4*4L screws.



5. Continue installing the outer rail bracket to the mounting frame. Attach the outer rail assembling to the frame and press the bracket to form a rack on both ends. Repeat to fully mount the bracket assembly on the other side.

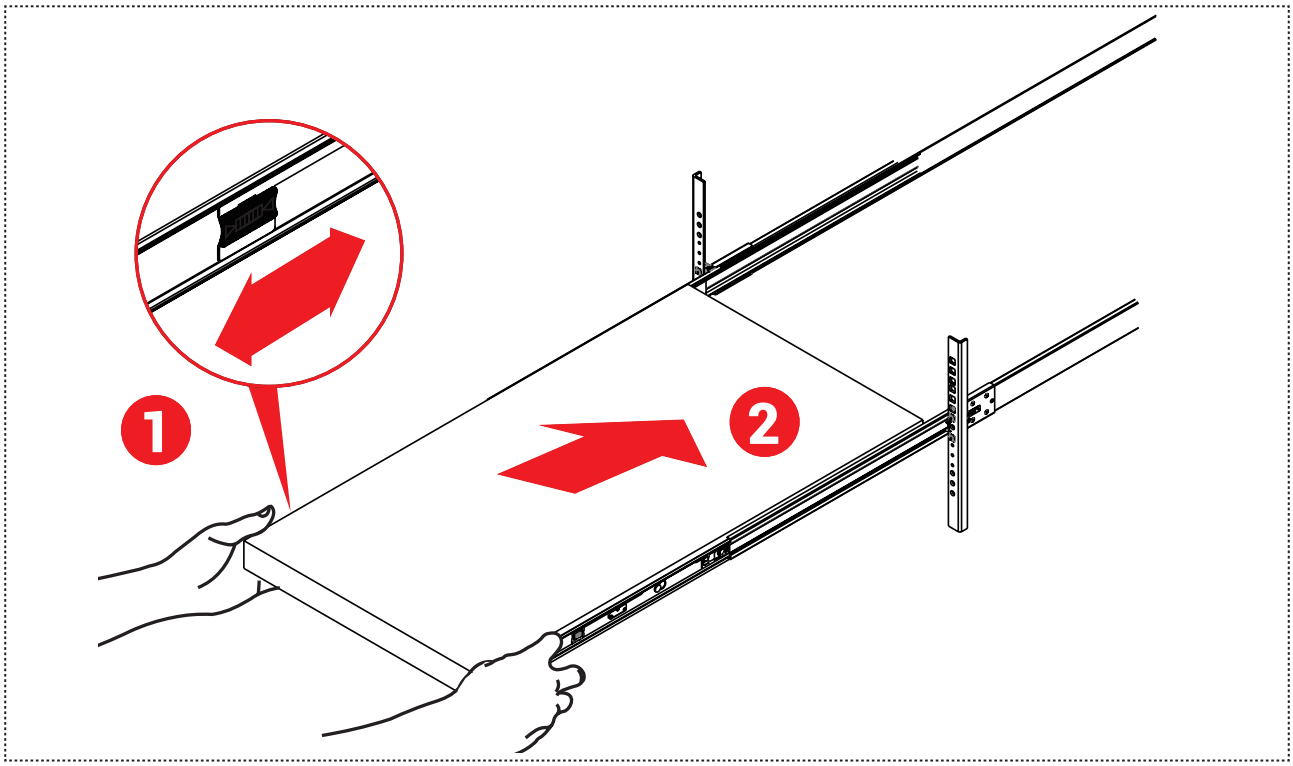


6. Pull out the middle channel until the ball bearing retainer is locked forward.



NOTE
Verify ball bearing retainer is locked forward.

7. Slide the release tab and push barebone into rack. Make sure the barebone is completely installed onto the rack.

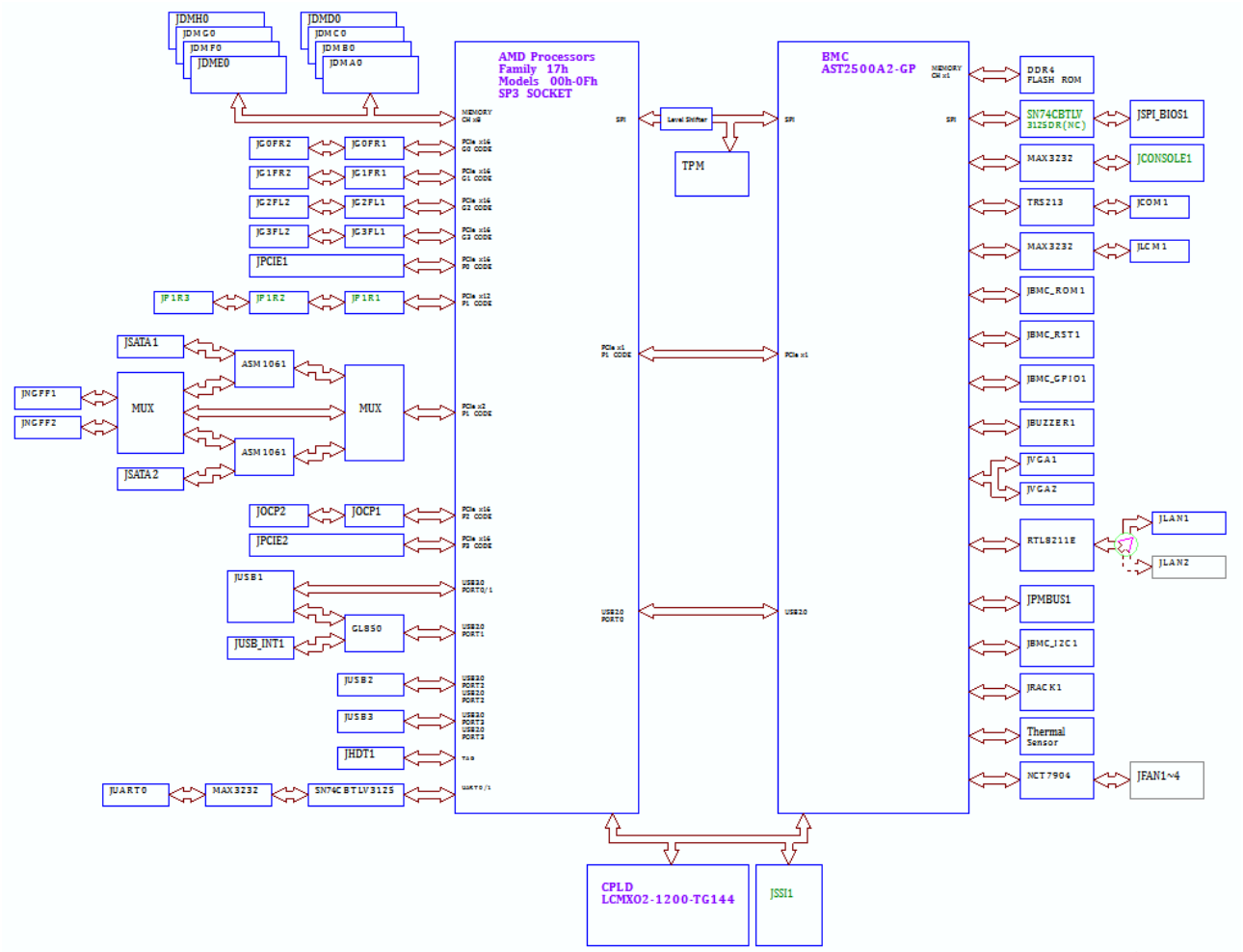


Chapter 3. Hardware Settings

This section provides illustrations that display the internal jumpers, connectors, and system LED indicators on the Auriga motherboard. The motherboard layout and essential connectors are listed below for your reference.

3.1 Motherboard

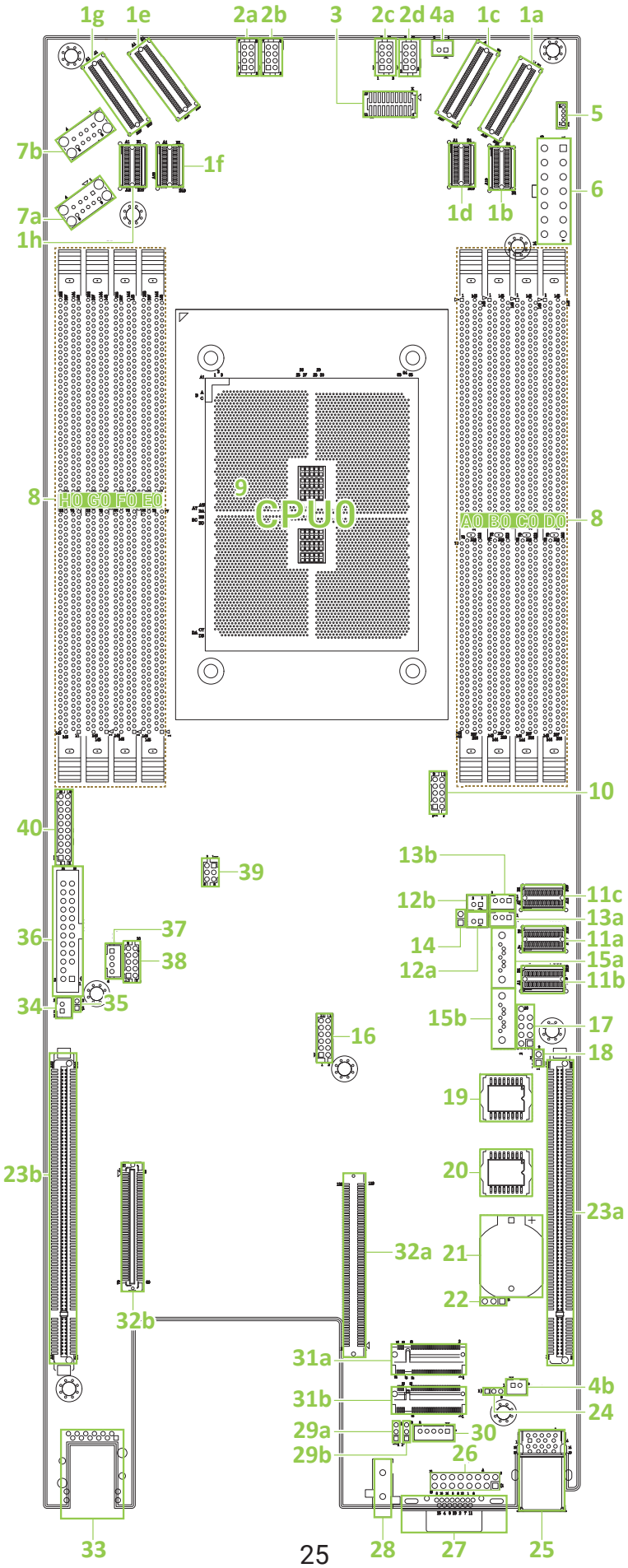
3.1.1 Block Diagram



3.1.2 Content List

Connector/Jumper/Header		Placement	Connector/Jumper/Header		Placement
1a 1b 1c 1d 1e 1f 1g 1h	PCIe Bus SAS slimline Connector	JG0FR1 JG0FR2 JG1FR1 JG1FR2 JG2FL1 JG2FL2 JG3FL1 JG3FL2	21	Battery Socket (For CR2032)	JBAT1
2a 2b 2c 2d	Fan Header	JFAN1 JFAN2 JFAN3 JFAN4	22	SOC CMOS Clear Jumper	JCMOS1
3	HDT Connector	JHDT1	23a 23b	Standard PCIe slot x16	JPCIE1 JPCIE2
4a 4b	Remote Thermal Sensor Connector	JTHM1 JTHM2	24	BMC Debug Port Header	JBMC_DP1
5	PMBUS I²C Header	JPMBUS1	25	External USB2.0/3.0 x2 Connector	JUSB1
6	Power Supply Connector	JPWR1	26	Front VGA Header	JVGA2
7a 7b	Internal USB2.0/3.0 Type-A Vertical Connector	JUSB2 JUSB3	27	External VGA Connector	JVGA1
8	DIMM Slot	JDMA0, JDMB0, JDMC0, JDMD0, JDME0, JDMF0, JDMG0, JDMH0	28	BMC Console Port	JCONSOLE1
9	CPU Socket	JCPU0	29a 29b	BMC Console Port Select Header	J3 J4
10	SOC UART Header	JUART0	30	Front Plane Controller Header	JLCM1
11a 11b 11c	PCIe Bus SAS slimline Connector	JP1R1 JP1R2 JP1R3 (Reserve)	31a 31b	NGFF(M.2) Connector	JNGFF1 JNGFF2
12a 12b	SATA DOM Power Jumper	JSATA1_PWR1 JSATA2_PWR1	32a 32b	OCP Connecter	JOCP1 JOCP2
13a 13b	SATA DOM Power Jumper	JSATA1_PWR2 JSATA2_PWR2	33	RJ45 Connector	JLAN1
14	BMC Reset Jumper	JBMC_RST1	34	Chassis Intrusion Header	JINTRUDER1
15a 15b	SATA HDD Connector	JSATA1 JSATA2	35	BMC Buzzer Header	JBUZZER1
16	LPC Debug Port Header	JLPC1	36	SSI Front panel Header	JSSI1
17	Front I/O USB Header	JUSB_INT1	37	IPMB PMBus Header	JBMC_I2C1
18	BMC Enable/Disable Jumper	JBMC_DIS1	38	BMC COM2 Header	JCOM1
19	BMC Firmware ROM Socket	JBMC_ROM1	39	GPIO Header	JBMC_GPIO1
20	System BIOS ROM Socket	JSPI_BIOS1	40	Front panel Header for Rack	JRACK1

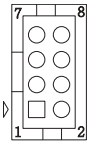
3.1.3 Connector and Junper Placement



3.1.4 Connector and Junper Pin Define

2a Fan Header (JFAN1)

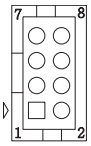
2x4-pin header that connects fan 1.



FANTACH_2	1	2	FANTACH_1
+12V_S0	3	4	+12V_S0
SYS1_FAN_PWM_C	5	6	SYS1_FAN_PWM_C
GND	7	8	GND

2b Fan Header (JFAN2)

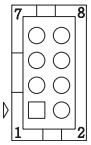
2x4-pin header that connects fan 2.



FANTACH_4	1	2	FANTACH_3
+12V_S0	3	4	+12V_S0
SYS2_FAN_PWM_C	5	6	SYS2_FAN_PWM_C
GND	7	8	GND

2c Fan Header (JFAN3)

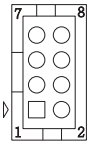
2x4-pin header that connects fan 3.



FANTACH_6	1	2	FANTACH_5
+12V_S0	3	4	+12V_S0
SYS3_FAN_PWM_C	5	6	SYS3_FAN_PWM_C
GND	7	8	GND

2d Fan Header (JFAN4)

2x4-pin header that connects fan 4.



FANTACH_8	1	2	FANTACH_7
+12V_S0	3	4	+12V_S0
SYS4_FAN_PWM_C	5	6	SYS4_FAN_PWM_C
GND	7	8	GND

4a Remote Thermal Sensor Connector (JTHM1)

2-pin header employed for monitoring temperature.

1	HM_TD4+
2	HM_TD4-

4b Remote Thermal Sensor Connector (JTHM2)

2-pin header employed for monitoring temperature.

1	HM_TD2+
2	HM_TD2-

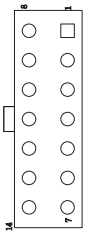
5 PMBUS I²C Header (JPMBUS1)

5-pin header for power management

1	SMB_PMBUS_CLK
2	SMB_PMBUS_DATA
3	PMBUS_ALERT_N
4	GND
5	+3V3_S5

6 Power Supply Connector (JPWR1)

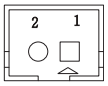
2x7-pin connector for main power supply.



+12V_S0	8	1	GND
+12V_S0	9	2	GND
+12V_S0	10	3	GND
+12V_S0	11	4	GND
+12V_S0	12	5	GND
+5V_STBY_PSU	13	6	GND
PS_OK_12V	14	7	PS_ON_12V_N

12a SATA-DOM Power Jumper (JSATA1_PWR1)

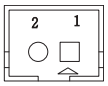
2-pin that supplies power to SATA DOM.



1	+5V_S0_SATA1
2	GND

12b SATA-DOM Power Jumper (JSATA2_PWR1)

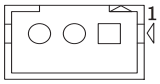
2-pin that supplies power to SATA DOM.



1	+5V_S0_SATA2
2	GND

13a SATA-DOM Power Jumper (JSATA1_PWR2)

3-pin that supplies power to SATA DOM.

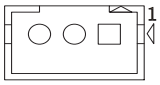


1	GND
2	DOM_PWR1
3	+5V_S0_SATA1

Jumper default Pin-1 & Pin-2

13b SATA-DOM Power Jumper (JSATA2_PWR2)

3-pin that supplies power to SATA DOM.

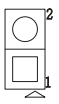


1	GND
2	DOM_PWR2
3	+5V_S0_SATA2

Jumper default Pin-1 & Pin-2

14 BMC Reset Jumper (JBMC_RST1)

2-pin for resetting BMC jumper.

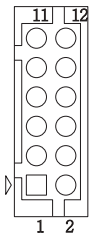


1	BMC_RESET (BMC SRST#)
2	GND

Jumper default OPEN

16 LPC Debug Port Header (JLPC1)

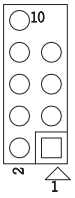
2x6-pin header for low pin count debug.



LPC_HDR_CLK	2	1	GND
P0_LFRAME_N	4	3	P0_LDRQ0_N
LPC_HDR_RST_N	6	5	P0_SERIRQ
P0_LAD3	8	7	P0_LAD2
+3V3_S0	10	9	P0_LAD1
P0_LAD0	12	11	GND

7 Front I/O USB Header (JUSB_INT1)

9-pin USB header for the front panel.



+5V_HUB2	1	2	+5V_HUB2
USB2_HUB1_DN	3	4	USB2_HUB2_DN
USB2_HUB1_DP	5	6	USB2_HUB2_DP
GND	7	8	GND
KEY (no pin)	9	10	GND

18 BMC Enable/Disable Jumper (JBMC_DIS1)

2-pin jumper that enables/ disables BMC.

1	FW_SPI_CS0_N
2	GND

Jumper default keep OPEN.

22 SOC CMOS Clear Jumper (JCMOS1)

3-pin jumper to reset BIOS setting.

1	+VDDBT_RTC_JP (CR2032)
2	+1V5_RTC (SOC)
3	GND

Jumper default Pin-1 & Pin-2

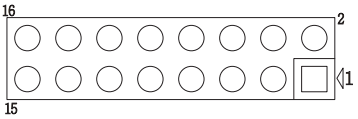
24 BMC Debug Port Header (JBMC_DP1)

3-pin header for BMC debug.

1	RS232_TXD5
2	RS232_RXD5
3	GND

26 Front VGA Header (JVGA2)

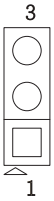
2x8-pin VGA header for front panel.



DACROA	2	1	GND
NC	4	3	DACGOA
GND	6	5	DDC_DATAO
DACBOA	8	7	GND
AHSYNCO	10	9	NC
DVO_5V	12	11	AVSYNCO
GND	14	13	GND
DDC_CLKO	16	15	GND

29a BMC Console Port Select Header (J3)

3-pin header for selecting BMC console.

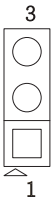


1	TX1
2	PJ_TX
3	TX5

Jumper default Pin-1 & Pin-2

29b BMC Console Port Select Header (J4)

3-pin header for selecting BMC console.

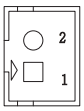


1	RX1
2	PJ_RX
3	RX5

Jumper default Pin-1 & Pin-2

34 Chassis Intrusion Header (JINTRUDER1)

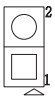
2-pin header for detecting the chassis of being opened.



1	CHASSIS_OPEN_N
2	GND

35 BMC Buzzer Header (JBUZZER1)

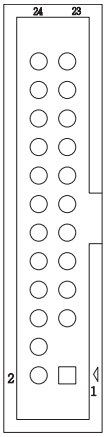
2-pin internal buzzer/speaker header for BMC.



1	+5V_S0
2	BMC_BUZZER

36 SSI Front panel Header (JSSI1)

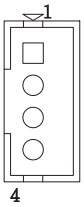
2x12-pin header for SSI front panel cable.



FP_HDR_PWR_LED	1	2	FP_PWR (+3V3_S5)
KEY (no pin)	3	4	HDR_CHASSIS_ID_LED (+5V_S5)
FP_PWR_LED_L	5	6	ID_LED_OUT_N
HDD_LED_P (+3V3_S5)	7	8	SYS_HEALTH2#
HDD_LED_N	9	10	SYS_HEALTH#
FP_PWR_BTN_N	11	12	LAN1_ACTLED_PWR
GND	13	14	PHY1_LED0_N
SW_COLD_RST_N	15	16	BMC_I2C_08_SDA
GND	17	18	BMC_I2C_08_SCL
BMC_ID_IN_N	19	20	CHASSIS_OPEN
TEMP_SENSOR (NC)	21	22	LAN2_ACTLED_PWR
FP_NMI_BTN_N	23	24	PHY1_LED1_R

37 IPMB PMBus Header (JBMC_I2C1)

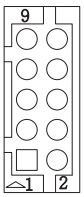
4-pin power management header for BMC.



1	BMC_I2C_01_SDA
2	GND
3	BMC_I2C_01_SCL
4	NC

38 BMC COM2 Header (JCOM1)

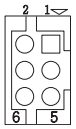
2x5-pin COM2 header for BMC.



DCDB	2	1	DSRB
RXDB	4	3	RTSB
TXDB	6	5	CTSB
DTRB	8	7	RIB
GND	10	9	NC

39 GPIO Header (JBMC_GPIO1)

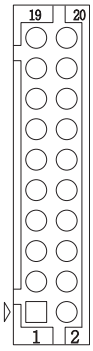
2x3-pin GPIO BMC header.



RACK_EXTRST_N	2	1	GND
BMC_GPY1	4	3	BMC_I2C_09_SDA
BMC_GPY0	6	5	BMC_I2C_09_SCL

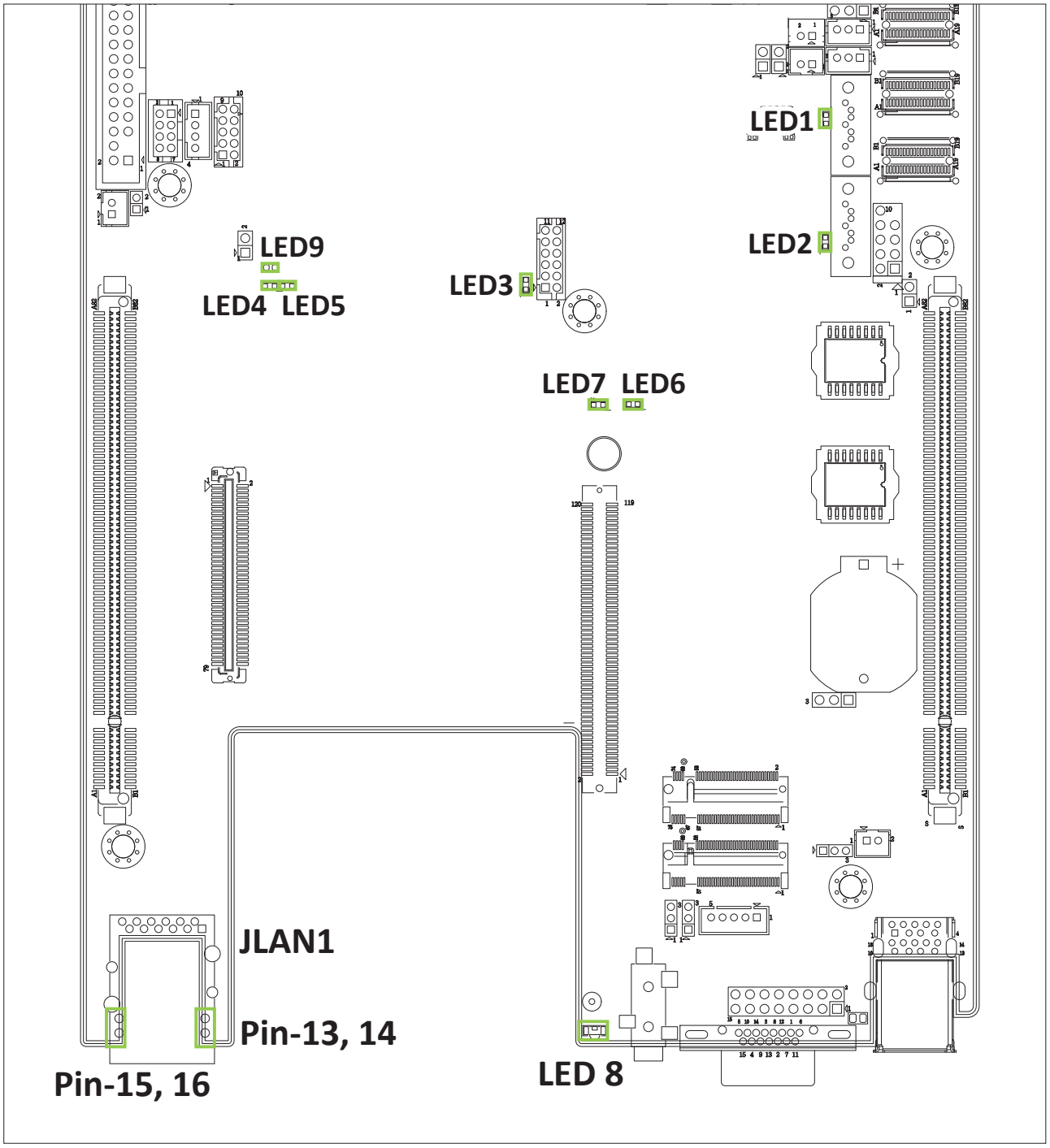
40 Front panel Header for RACK (JRACK1)

2x10-pin front panel header for rack connection.



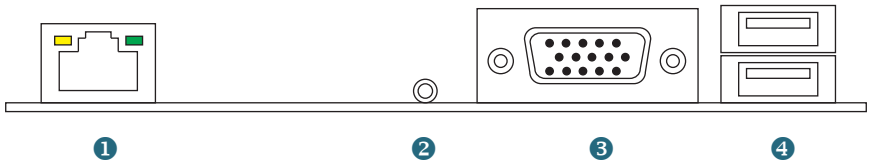
RACK_EXTRST_N	1	2	BMC_I2C_08_SCL
GND	3	4	BMC_I2C_08_SDA
BMC_I2C_01_SCL	5	6	GND
BMC_I2C_01_SDA	7	8	RACK_PWM0
GND	9	10	RACK_TACH0
RACK_PMBUS _CLK	11	12	GND
RACK_PMBUS _DATA	13	14	RACK_PWM1
PMBUS_ALERT_N	15	16	RACK_TACH1
RACK_CHASSIS_ OPEN	17	18	RACK_GPIO_EXIN
GND	19	20	CHASSIS_1U2N_N

3.1.5 Internal LED



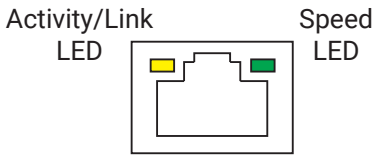
LED1	JSATA1 status LED (U2005 ASM1061)	On (Blinking)	Indicates SATA is in use when LED is lit.
		Off	Indicates SATA is un-used when LED is dark.
LED2	JSATA2 status LED (U2008 ASM1061)	On (Blinking)	Indicates SATA is in use when LED is lit.
		Off	Indicates SATA is un-used when LED is dark.
LED3	HEART BEAT	On (Blinking)	BMC activity is detected.
		On	BMC is not active.
LED6	RSMRST LED	On	Resume Well Reset is ready.
		Off	Resume Well Reset is not ready.
LED7	POWER GOOD LED	On	System power good is ready.
		Off	System power good is not ready.
LED4, LED9	LAN Speed LED (JLAN1, 15, 16)	On	LAN Linking Speed : (1) 1Gbps : Green (LED9) (2) 100Mbps : Amber (LED4)
		Off	(1) LAN Linking Speed 10Mbps (2) No connection
LED5	LAN status LED (JLAN1,13,14)	On (Blinking)	LAN Cable Linking Status
		Off	LAN* is not active and the LAN cable is not connected.
LED8	UID LED	On (Blinking)	UID activity is detected.
		Off	UID activity is not detected.

3.1.6 Rear I/O Panel



Item	Placement	Item	Placement
1	LAN RJ45 Port	3	VGA port
2	COM port by 3.5mm phone jack	4	USB 2.0/3.0 Port *2

LAN LED

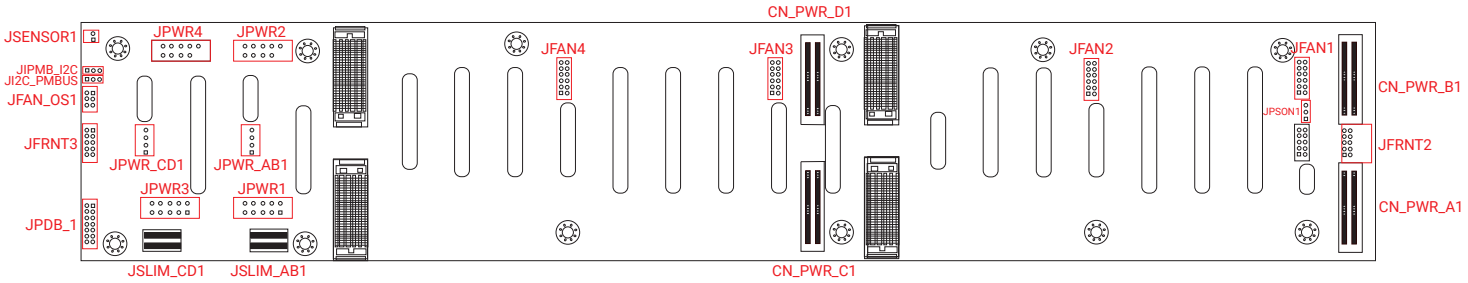


Item	Color	Behavior
Activity/Link LED	Off	No link.
	Yellow (blinking)	Data activity.
	On	Link.
Speed LED	Off	10M bps connection or no link.
	Off	100M bps connection.
	Green	1G bps connection.

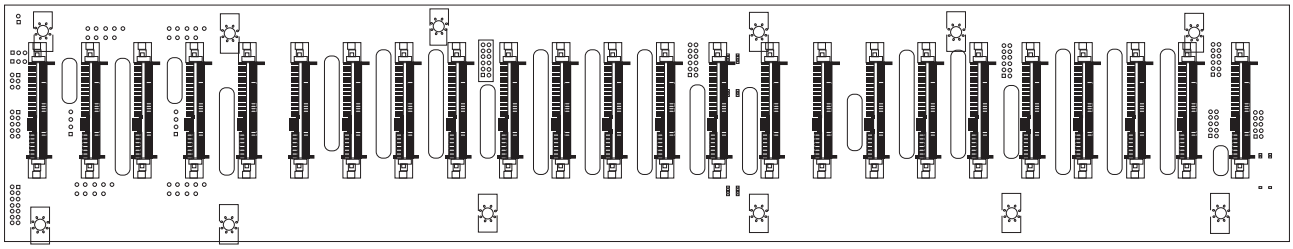
3.2 SAS/U.2 Drive Backplane

3.2.1 Placement

Top View

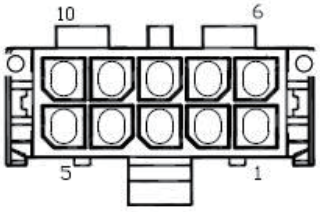


Bottom View



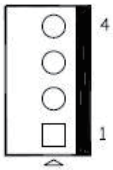
3.2.2 Connector and Jumper

Power Input Connector (JPWR1, JPWR2, JPWR3, JPWR4)



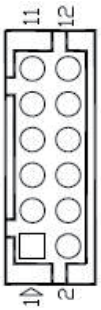
+12V	6	1	GND
+12V	7	2	GND
+12V	8	3	GND
+12V	9	4	GND
+12V	10	5	GND

Power Output Connector (JPWR_AB1, JPWR_CD1)



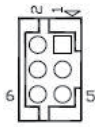
1	+12V
2	GND
3	GND
4	+5V

Fan Connector (JFAN1, JFAN2, JFAN3, JFAN4)



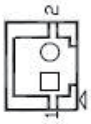
FAN_TACH1/3/5/7	1	2	FAN_TACH2/4/6
+12V	3	4	+12V
+12V	5	6	+12V
GND	7	8	GND
GND	9	10	GND
PWM_AB/PWM_CD	11	12	GND

OS Fan Connector (JFAN_OS1)



OS_FAN_TACH1	1	2	OS_FAN_TACH2
+12V	3	4	+12V
OS_PWM	5	6	GND

Thermal Sensor Connector (JSENSOR)



1	DP
2	DN

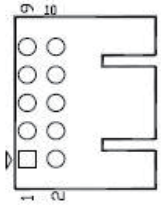
IPMB External Connector (JIPMB_I2C)

1	IPMB_SCL
2	GND
3	IPMB_SDA

PMBUS External Connector (JI2C_PMBUS)

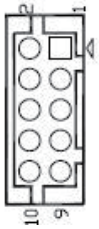
1	BMC_I2C6_SCL
2	GND
3	BMC_I2C6_SDA

Front I/O Header (JFRONT2)



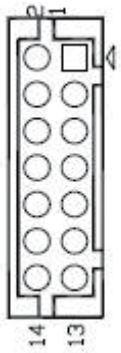
B_PWR_BTN	2	1	A_PWR_BTN
B_POWER_ON_LED	4	3	A_POWER_ON_LED
B_SYS_LED_FAULT	6	5	A_SYS_LED_FAULT
B_ID_LED	8	7	A_ID_LED
GND	10	9	GND

Front I/O Header (JFRONT3)



D_PWR_BTN	2	1	C_PWR_BTN
D_POWER_ON_LED	4	3	C_POWER_ON_LED
D_SYS_LED_FAULT	6	5	C_SYS_LED_FAULT
D_ID_LED	8	7	C_ID_LED
GND	10	9	GND

PDB Function I/F (JPDB_1)



BMC_I2C6_SCL	2	1	PSU_PON
BMC_I2C6_SDA	4	3	POWER_OK
PSU_PRSENT_1	6	5	PMBUS_ALERT
PSU_PRSENT_2	8	7	GND
+12VSTBY	10	9	GND
+12VSTBY	12	11	GND
+12VSTBY	14	13	GND

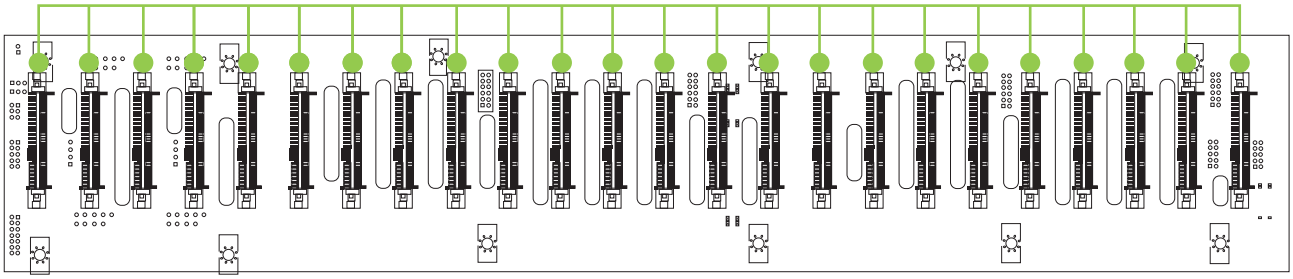
PS_ON Mode Selection (JPSON1)

POWER_ON		
PSU_PON	ATX Mode	Pin 1,2 Close
GND	AT Mode	Pin 2,3 Close

3.2.3 Cable Routing

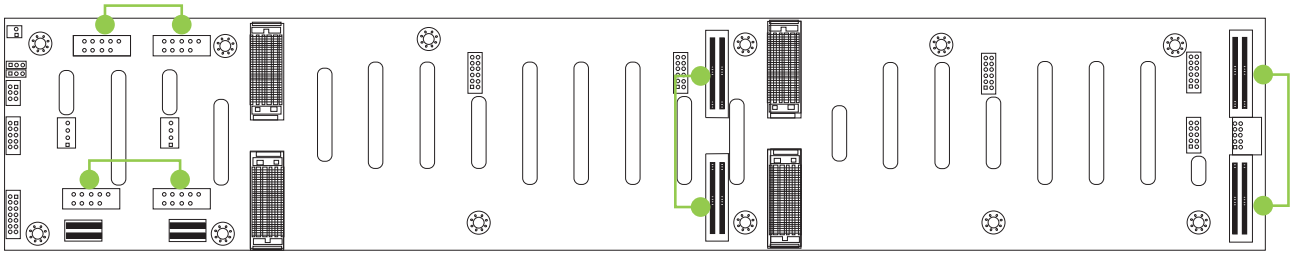
Top view

Connects to SATA/U.2 storage device



Bottom view

Connects four 10-pin plug from motherboard



Connects the data cable to motherboard

Chapter 4. BIOS Configuration Settings

This chapter demonstrates how to configure the UEFI BIOS settings in your system device. You can enter the BIOS screen during system startup.

To enter BIOS configuration settings,
- Press **Esc** key during the Power-On-Self-Test (POST)

To enter BIOS after POST, you have to restart the system by using one of the three methods:
- Press **Ctrl** + **Alt** + **Delete**.
- Press the reset button on the system chassis.
- Turn the system off and on.

NOTE
The following pages provide the details of BIOS menu. Please notice that the BIOS menu are continually changing due to the BIOS update. The BIOS menu provided are the most updated ones when this manual is written.

NOTE
For further details about the BIOS, please refer to BIOS section in the Auriga manual for reference. AIC® website link: https://www.aicipc.com/en/productdetail/50929.

4.1 Navigation Keys

The navigation keys are listed below.

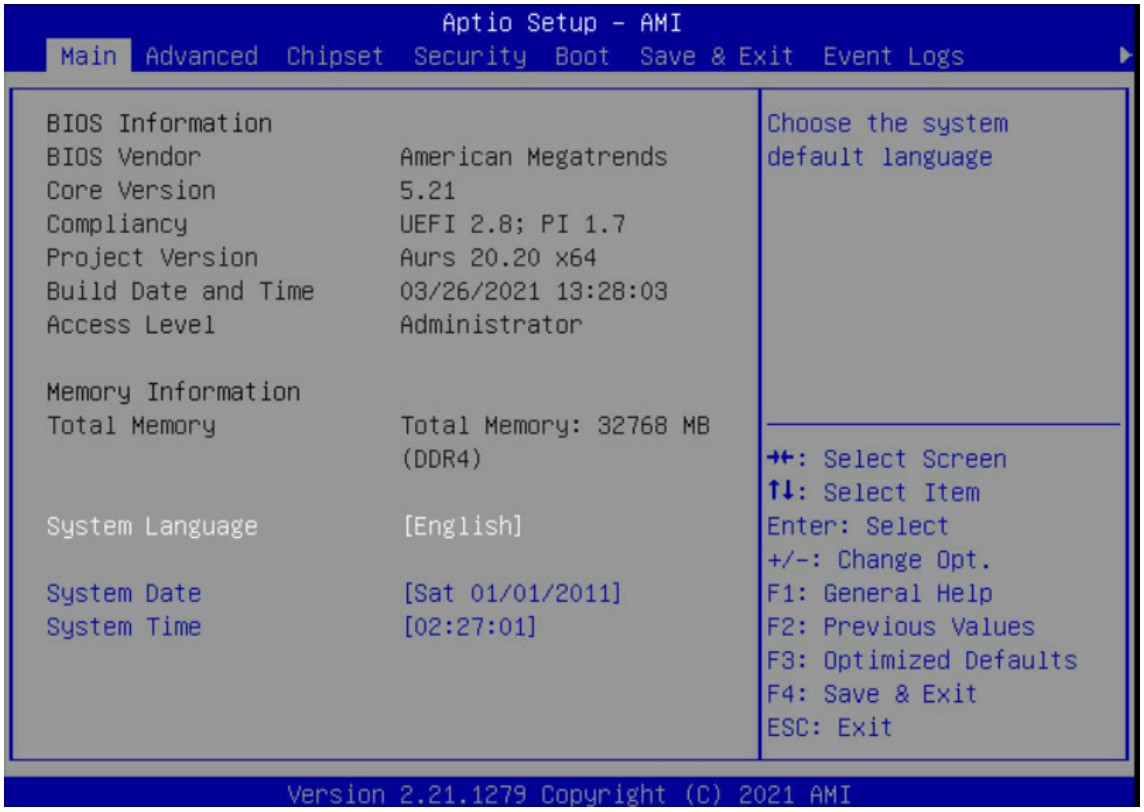
Function Key	Description
< ↑ > < ← > < → > < ↓ >	Select item.
< Enter >	Select and enter sub-screen.
< + > < - >	Modify selected option.
< F1 >	General help.
< F2 >	Previous Value.
< F3 >	Optimized defaults.
< F4 >	Save & Exit.
< F5> < F6 >	Change values.
< F7 >	Discard Change and Exit.
< F9 >	Load Optimal Default for all values.
< F10 >	Save changes and exit.
< F12 >	Print Screen.
< Esc >	Exit the current menu screen.

4.2 Menu

Press ⬅ and ➡ to select the options of the menu bar.
Press **Enter** to access the option screen.

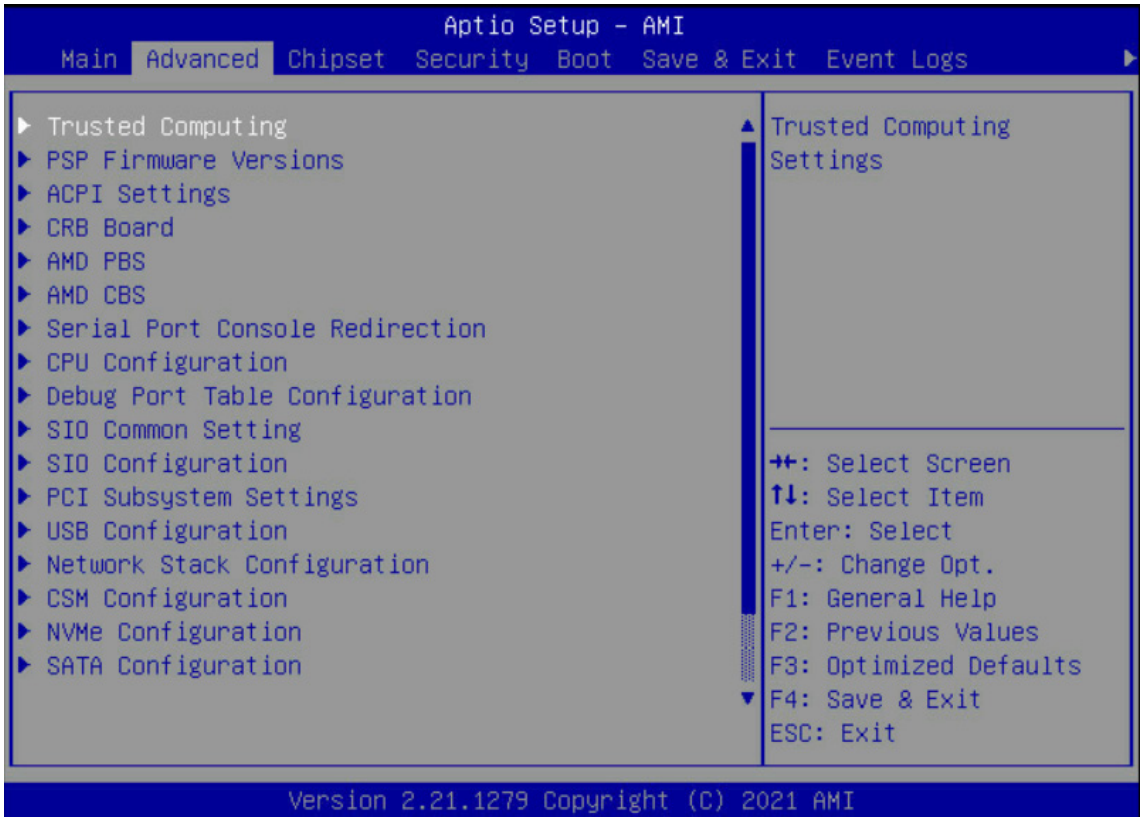
Menu	Description
Main	Displays system information such as CPU bus speed, system memory speed, total installed memory, current EFI language, and system date & time.
Advanced	Allows configuration of advanced system settings such as ACPI features, boot, and chipset configuration.
Chipset	View the configuration of server chipsets.
Security	Sets passwords and security functions.
Boot	Sets boot options such as Quick Boot or USB Boot.
Save and Exit	Save changes and exit, discard changes and exit, discard changes, or load optimal or fail-safe defaults.
Event Logs	Displays the configurations of SMBios Event Logs.
Server Management	Allows configuration of timer, System Event Log, and BMC network.

4.3 Main



Main	
System Language	Configures the language used in the system.
System time	Configures the current time.
System date	Configures the current date.

4.4 Advanced



4.4.1 Trusted Computing

Trusted Computing settings.

Trusted Computing			
Security Device Support	Enable		Disable
SHA-1/256/384 PCR Bank	Enable		Disable
Pending operation	None		TPM Clear
Platform Hierarchy	Enable		Disable
Storage Hierarchy	Enable		Disable
Endorsement Hierarchy	Enable		Disable
TPM 2.0 UEFI Spec Version	TCG_1_2		TCG_2
Physical Presence Spec Version	1.2		1.3
Device Select	Auto	TPM 1.2	TPM 2.0

4.4.2 ACPI Settings

System ACPI parameters.

ACI Settings		
Enable ACPI Auto Configuration	Enable	Disable

4.4.3 AMD PBS

AMD PBS setup page.

AMD PBS				
RAS	RAS Periodic SMI Control	Enable	Disable	
	SMI Threshold	5		
	SMI Scale	1000		
	SMI Scale Unit	millisecond	second	minute
	SMI Period	1000		
	GHES Notify Type	Polled	SCI	
	GHES UnCorr Notify Type	Polled	NMI	
	PCIe GHES Notify Type	Polled	SCI	
	PCIe UnCorr GHES Notify Type	Polled	NMI	
	PCIe Root Port Corr Err Mask Reg	0		
	PCIe Root Port Un Corr Err Mask Reg	0		
	PCIe Root Port Un Corr Error Sev Reg	7EF6030		
	PCIe Device Corr Err Mask Reg	0		
	PCIe Device Un Corr Err Mask Reg	100000		
	PCIe Device Un Corr Error Sev Reg	7EF6030		
	CCIX GHES Deffered Err Notify Type	Polled	SCI	
	CCIX GHES Corrected Err Notify Type	Polled	SCI	
	DDR4 DRAM Hard Post Package Repair	Enable	Disable	
	HEST DMC Structure Support	Enable	Disable	
	RAS EINJ Mode	BIOS	PSP	
SPI Locking	Enable	Disable		
iLA Trace Memory En	Enable	Disable		

4.4.4 AMD CBS

AMB CBS setup page.

AMD CBS					
CPU Common Options	Performance	OC Mode	Normal Operation	Customized	
		SMT Control	Auto	Enable	Disable
	Prefetcher settings	L1/2 Stream HW Prefetcher	Auto	Enable	Disable
		L1 Stride Prefetcher	Auto	Enable	Disable
		L1 Region Prefetcher	Auto	Enable	Disable
		L2 Up/Down Prefetcher	Auto	Enable	Disable
	Core Watchdog	Core Watchdog Timer Enable	Auto	Enable	Disable
	Redirect For Return Dis	Auto	0	1	

CPU Common Options	Platform First Error Handling	Auto	Enable	Disable		
	Core Performance Boost	Auto	Enable	Disable		
	Global C-state Control	Auto	Enable	Disable		
	Power Supply Idle Control	Auto	Low Current Idle	Typical Current Idle		
	SEV ASID Count	Auto	253 ASIDs	509 ASIDs		
	SEV-ES ASID Space Limit Control	Auto	Manual			
	Streaming Stores Control	Auto	Enable	Disable		
	Local APIC Mode	Auto	xAPIC	x2APIC		
	ACPI _CST C1 Declaration	Auto	Enable	Disable		
	MCA error thresh enable	Auto	True	False		
	SMU and PSP Debug Mode	Auto	Enable	Disable		
	Xtrig7 Workaround	Auto	No Workaround	Bronze Workaround	Silver Workaround	
	PPIN Opt-in	Auto	Enable	Disable		
	SNP Memory (RMP Table) Coverage	Auto	Enable	Disable	Custom	
	SMEE	Auto	Enable	Disable		
	Action on BIST Failure	Auto	Do nothing	Down-CCD		
	Fast Short REP MOVSB	Enable	Disable			
	Enhanced REP MOVSB/STOSB	Enable	Disable			
	REP-MOV/STOS Streaming	Enable	Disable			
	X3D	Auto	Disable	1 stack	2 stacks	3 stacks
	IBS hardware workaround	Auto	Enable			
DF Common Options	Scrubber	DRAM Scrub time	Auto	1 hour	4 hours	8 hours
			Disable	16 hours	24 hours	48 hours
		Poison scrubber control	Auto	Enable	Disable	
		Redirect scrubber control	Auto	Enable	Disable	
		Redirect scrubber limit	Auto	Infinite	2	4	8
	Memory Addressing	NUMA nodes per socket	Auto	NPS2	NPS4	
		Memory interleaving	Auto	Disable		
		Memory interleaving size	Auto	256 Bytes	512 Bytes	1 KB	2 KB
		1TB remap	Auto	Do not remap	Attempt to remap	
		DRAM map inversion	Auto	Enable	Disable	
		Location of private memory regions	Auto	Distributed	Consolidated	Consolidated to 1st DRAM pair

DF Common Options	ACPI	ACPI SRAT L3 Cache As NUMA Domain	Auto				Enable				Disable				
		ACPI SLIT Distance Control	Auto								Manual				
		ACPI SLIT remote relative distance	Auto				Near				Far				
	Link	GMI encryption control	Auto				Enable				Disable				
		xGMI encryption control	Auto				Enable				Disable				
		CAKE CRC perf bounds Control	Auto								Manual				
		xGMI Link Configuration	Auto				2 xGMI Links				3 xGMI Links				4 xGMI Links
		4-link xGMI max speed (Gbps)	Auto		6.4		7.467		8.533		9.6				
			10.667	11	12	13	14	15	16	17					
			18	19	20	21	22	23	24	25					
		3-link xGMI max speed	Auto		6.4		7.467		8.533		9.6				
			10.667	11	12	13	14	15	16	17					
			18	19	20	21	22	23	24	25					
		xGMI TXEQ Mode	Auto				TXEQ_Lane				TXEQ_Link				TXEQ_RX_Vet
		xGMI 18GACOFC	Auto				Enable				Disable				
	Disable DF to external IP Sync Flood Propagation		Auto				Sync flood enable				Sync flood disable				
	Disable DF sync flood propagation		Auto				Sync flood enable				Sync flood disable				
	Frees of DF module		Auto				Enable				Disable				
	CC6 memory region encryption		Auto				Enable				Disable				
	System probe filter Memory Clear		Auto				Enable				Disable				
	Memory Clear		Auto				Enable				Disable				
	PSP error injection suport		True								False				
UMC Common Options	DDR4 Common Options	DRAM Controller Configuration	DRAM Power Options				Power Down Enable				Auto				
											Enable				
							Power Down Entry Delay				BB8				
							Sub Urg Ref Lower Bound				4				
							DRAM Maximum Activate Count				Auto				
											200 K				
											300 K				
											400 K				
											500 K				
											600 K				
											700 K				
											Untested MAC				
											Unlimited MAC				

UMC Common Options	DDR4 Common Options	DRAM Controller Configuration	DRAM Power Options	DRAM Refresh Rate	7.8 usec	
					3.9 usec	
				Self-Refresh Exit Staggering	Trfc / 3	
					Trfc / 4	
					Disable	
			Cmd2T	Auto	1T	2T
			Gear Down Mode	Auto	Enable	Disable
			CAD Bus Timin User Controls	Auto	Manual	
			CAD Bus Drive Strength User Controls	Auto	Manual	
		Data Bus Configuration	Data Bus Configuration User Controls	Auto	Manual	
		Common RAS	Data Poisoning	Auto	Enable	Disable
			DRAM Post Package Repair	Enable	Disable	
			RCD Parity	Auto	Enable	Disable
			DRAM Address Command Parity Retry	Auto	Enable	Disable
			Disable Memory Error Injection	True	False	
			ECC Configuration	DRAM ECC Symbol Size	Auto	x4
					x8	x16
				DRAM ECC Enable	Auto	
					Enable	
					Disable	
				DRAM UECC Retry	Auto	
					Enable	
					Disable	
		Security	TSME	Auto	Enable	Disable
			Data Scramble	Auto	Enable	Disable
		Phy Configuration	PMU Training	DFE Read Training	Auto	
					Enable	
					Disable	
				FFE Write Training	Auto	
					Enable	
					Disable	
				PMU Pattern Bits Control	Auto	Manual
	DRAM Memory Mapping	Chip Select Interleaving	Auto	Disable		
		Bank Group Swap	Auto	Enable	Disable	
		Bank Group Swap Alt	Auto	Enable	Disable	
		Address Hash Bank 2 ColXor	3F8			
		Address Hash Bank	Auto	Enable	Disable	

UMC Common Options	DRAM Memory Mapping	Address Hash CS	Auto	Enable	Disable	
		Address Hash Rm	Auto	Enable	Disable	
		SPD Read Optimization	Auto	Enable	Disable	
	NVDIMM	Disable NVDIMM-N Feature	No	Yes		
	Memory Bist	MBIST Enable	Enable	Disable		
		Data Eye	Pattern Select	PRBS	SS0	Both
			Pattern Length	3		
			Aggressor Channel	1 Aggressor Channel	3 Aggressor Channels	
				7 Aggressor Channels	Disable	
			Aggressor Static Lane Control	Enable	Disable	
			Target Static Lane Control	Enable	Disable	
			Worst Case Margin Granularity	Per Chip Select	Per Nibble	
			Read Voltage Sweep Step Size	1	2	4
			Read Timing Sweep Step Size	1	2	4
			Write Voltage Sweep Step Size	1	2	4
			Write Timing Sweep Step	1	2	4
		Memory Healing BIST	Disable	BIOS Mem BIST	Self-Healing Mem BIST	BIOS and Self-Healing Mem BIST
NBIO Common Options	IOMMU	Auto	Enable	Disable		
	ACS Enable	Auto	Enable	Disable		
	PCIe ARI Support	Auto	Enable	Disable		
	PCIe ARI Enumeration	Auto	Enable	Disable		
	PCIe Ten Bit Tag Support	Auto	Enable	Disable		
	HD Audio Enable	Auto	Enable	Disable		
	SMU Common Options	Determinism Control	Auto	Manual		
		Fan Control	Fan Table Control	Auto	Manual	
		cTDP Control	Auto	Manual		
		Efficiency Mode En	Auto	Enable		
		Package Power Limit Control	Auto	Manual		
		xGMI Link Width Control	Auto	Manual		
		APBDIS	Auto	0	1	
		DF Cstates	Auto	Enable	Disable	

NBIO Common Options	SMU Common Options	CPPC	Auto	Enable	Disable	
		HSMP Support	Auto	Enable	Disable	
		DLWM Support	Auto	Enable	Disable	
		Boost Fmax En	Auto	Manual		
		EDC Current Tracking	Enable	Disable		
		LCLK Frequency Control	Root Complex 0x00/0x40/ 0x80/0xC0 LCLK Frequency	Auto	593Mhz	
		DF Pstate Mode Select	Auto	Normal	Limit Highest	Limit All
	NBIO RAS Common Options	NBIO RAS Control	Auto	Disable	MCA	Legacy
		Egress Poison Severity High	30011			
		Egress Poison Severity Low	4			
		NBIO SyncFlood Generation	Auto	Enable	Disable	
		NBIO SyncFlood Reporting	Auto	Enable	Disable	
		Egress Poison Mask High	FFFCFFFF			
		Egress Poison Mask Low	FFFFFFFB			
		Uncorrected Converted to Poison Enable Mask High	30000			
		Uncorrected Converted to Poison Enable Mask Low	4			
		SLINK Read Response OK	Enable	Disable		
		SLINK Read Response Error Handling	Log Errors in MCA	Trigger MCOMMIT Error	Enable	
		Log Poison Data from SLINK	Enable	Disable		
		PCIe Aer Reporting Mechanism	Auto	Firmware First	OS First	
		Edpc Control	Auto	Enable	Disable	
		NBIO Poison Consumption	Auto	Enable	Disable	
		Sync Flood on PCIe Fatal Error	Auto	True	False	
	Enable AER Cap		Auto	Enable	Disable	
	Early Link Speed		Auto	Gen1	Gen2	
	Hot Plug Handling mode		Auto	Firmware First	OS First	
	Presence Detect Select mode		Auto	And	Or	
	Preferred IO		Auto	Bus		
	Data Link Feature Cap		Auto	Enable	Disable	

NBIO Common Options	CV test	Auto	Enable	Disable	
	SEV-SNP Support	Enable	Disable		
FCH Common Options	SATA Configuration Options	SATA Enable	Auto	Enable	Disable
		Sata RAS Support	Auto	Enable	Disable
		Sata Disabled AHCI Prefetch Function	Auto	Enable	Disable
		Aggressive SATA Device Sleep Port 0/1	Auto	Enable	Disable
		SATA Controller Options	SATA Controller Enable	Sata0-7 Enable	Auto
					Enable
					Disable
			SATA Controller DevSlp	Socket1 DevSlp	Auto
					Enable
					Disable
	SATA Configuration Options	SATA Controller Options	SATA Controller SGPIO	Sata0-7 SGPIO	Auto
					Enable
					Disable
	USB Configuration Options	XHCI Controller0/1 enable	Auto	Enable	Disable
		USB ecc SMI Enable	Auto	Enable	Off
		MCM USB enable	XHCI2/3 enable (Socket1)	Auto	
				Enable	
				Disable	
	SD Dump Options	SD Configuration Mode	SD Dump enable	SD Dump disable	
	AC Power Loss Options	Ac Loss Control	Auto	Previous	Reserved
			Always On	Always Off	
	I2C Configuration Options	I2C 0-5 Enable	Auto	Enable	Disable
	Uart Configuration Options	Uart 0-3 Enable	Auto	Enable	Disable
	FCH RAS Options	ALink RAS Support	Auto	Enable	Disable
		Reset after Sync flood	Auto	Enable	Disable
	Miscellaneous Options	Boot Timer Enable	Auto	Enable	Disable
	Socket-0 P0-3 NTB Enable	Auto	Enable		
	ABL Console Out Control	Auto	Enable	Disable	
	Workload Profile	Auto	CPU Intensive	Java Throughput	Java Latency
	Performance Tracing	Auto	Enable	Disable	

4.4.5 Serial Port Console Redirection

Serial Port Console Redirection.

Serial Port Console Redirection												
Console Redirection	Enable						Disable					
Console Redirection Settings	Terminal Type	ANSI		VT100			VT100+			VT-UTF8		
	Bits per second	9600		19200		38400		57600		115200		
	Data Bits	7					8					
	Parity	Even		Odd		Mark		Space		None		
	Stop Bits	1					2					
	Flow Control	None					Hardware RTS/CTS					
	VT-UTF8 Combo Key Support	Enable					Disable					
	Recorder Mode	Enable					Disable					
	Resolution 100x31	Enable					Disable					
	Putty Key Pad	VT100	LINUX		XTERMR6		SCO		ESCN		VT400	
Legacy Console Redirection Settings	Redirection COM Port	COM0					COM1					
	Resolution	80x24					80x25					
	Redirect After POST	Always Enable					Boot Loader					
Console Redirection EMS	Enable						Disable					

4.4.6 CPU Configuration

CPU configuration parameters.

CPU Configuration		
SVM Mode	Enable	Disable

4.4.7 Debug Port Table Configuration

Enables/disables DBGP and DBG2 Tables.

Debug Port Table Configuration		
Debug Port Table	Enable	Disable

4.4.8 SIO Common Setting

SIO Common setting.

SIO Common Setting		
Lock Legacy Resources	Enable	Disable

4.4.9 SIO Configuration

SIO configuration.

SIO Configuration				
[*Active*] Serial Port 1/2/3	Use This Device	Enable	Disable	
	Possible	Use Automatic Settings	IO=3F8h; IRQ=4; DMA	IO=3F8H; IRQ=3, 4, 5, 7, 9, 10, 11, 12; DMA;
		IO=2F8h; IRQ=3, 4, 5, 7, 9, 10, 11, 12; DMA;	IO=3E8H; IRQ=3, 4, 5, 7, 9, 10, 11, 12; DMA;	IO=2E8h; IRQ=3, 4, 5, 7, 9, 10, 11, 12; DMA;

4.4.10 PCI Subsystem Settings

PCI Subsystem settings.

PCI Subsystem Settings			
Above 4G Decoding	Enable	Disable	
	Enable	Disable	
SR-IOV Support	Enable	Disable	
BME DMA Mitigation	Enable	Disable	
Hot-Plug Support	Enable	Disable	
	Enable	Disable	
Onboard Device [Mass Storage Controller]	Disable Above 4G Decoding	Enable	Disable
	Disable PCI Init	Enable	Disable
	Disable PCIe GEN 2	Enable	Disable

4.4.11 USB Configuration

USB configuration parameters.

USB Settings					
Legacy USB Support	Auto	Enable	Disable		
XHCI Hand-off	Enable	Disable			
USB Mass Storage Driver Support	Enable	Disable			
Port 60/64 Emulation	Enable	Disable			
USB transfer time-out	1 sec	5 sec	10 sec	20 sec	
Device reset time-out	10 sec	20 sec	30 sec	40 sec	
Device power-up delay	Auto	Manual			
AMI Virtual CDROM0/1/2/3 1.00	Auto	Floppy	Forced FDD	Hard Disk	CD-ROM
AMI Virtual HDisk0/1/2/3 1.00	Auto	Floppy	Forced FDD	Hard Disk	CD-ROM
	Auto	Floppy	Forced FDD	Hard Disk	CD-ROM

4.4.12 Network Stack Configuration

Network Stack setting.

Network Stack Configuration		
Network Stack	Enable	Disable

4.4.13 CSM Configuration

Enables/disables Option ROM execution settings.

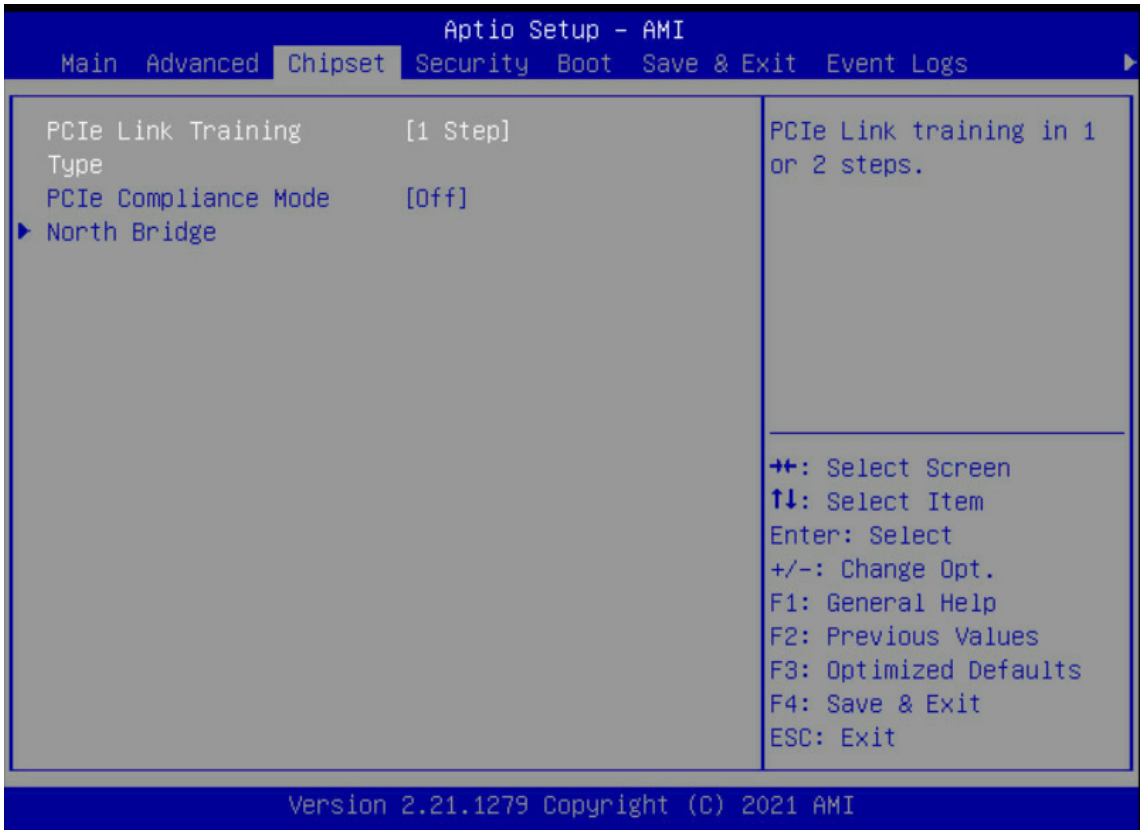
CSM Configuration			
CSM Support	Enable	Disable	
GateA20 Active	Upon Request	Always	
INT19 Trap Response	Immediate	Postponed	
Boot option filter	UEFI and Legacy	Legacy only	UEFI only
Network	UEFI	Legacy	Do not launch
Storage	UEFI	Legacy	Do not launch
Video	UEFI	Legacy	Do not launch
Other PCI devices	UEFI	Legacy	Do not launch
	UEFI	Legacy	Do not launch

4.4.14 T1s Auth Configuration

Select T1s Auth Configuration.

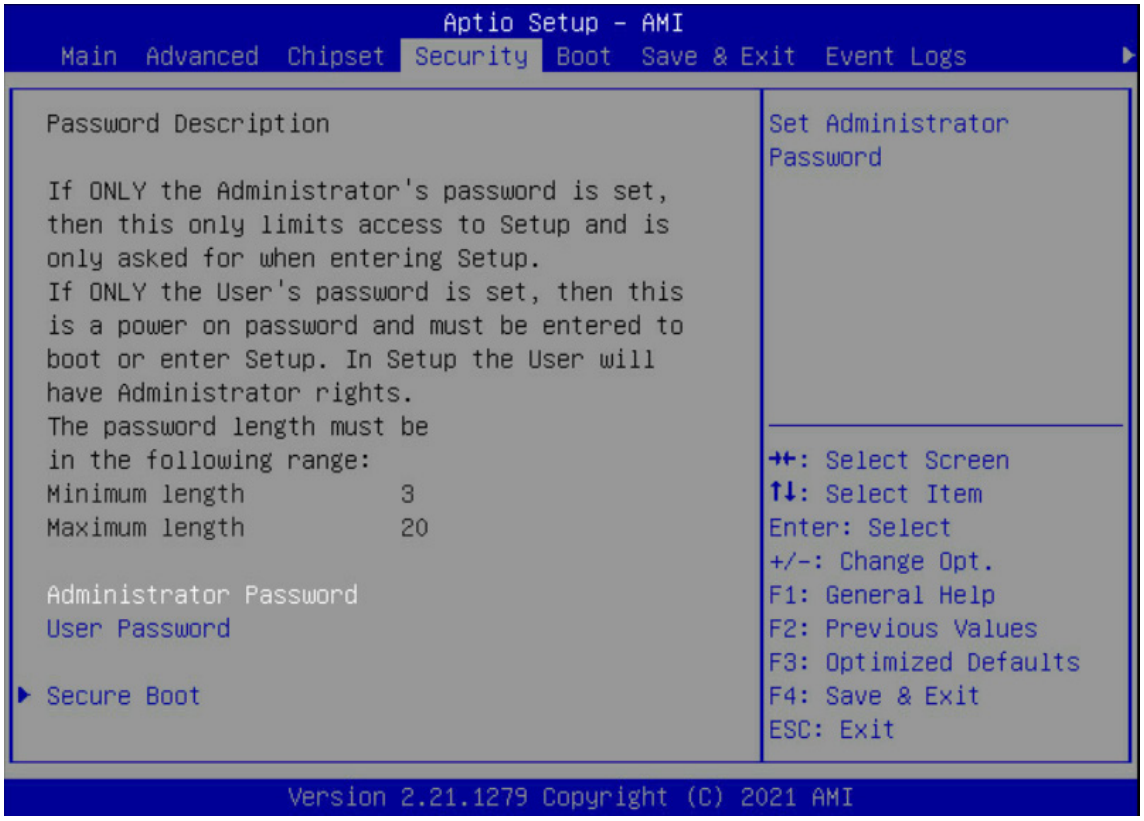
T1s Auth Configuration			
Server CA Configuration	Enroll Cert	Enroll Cert Using File	Enroll Cert using file.
		Commit Changes and Exit	Commit changes and exit.
		Discard Changes and Exit	Discard changes and exit.
	Delete Cert		

4.5 Chipset



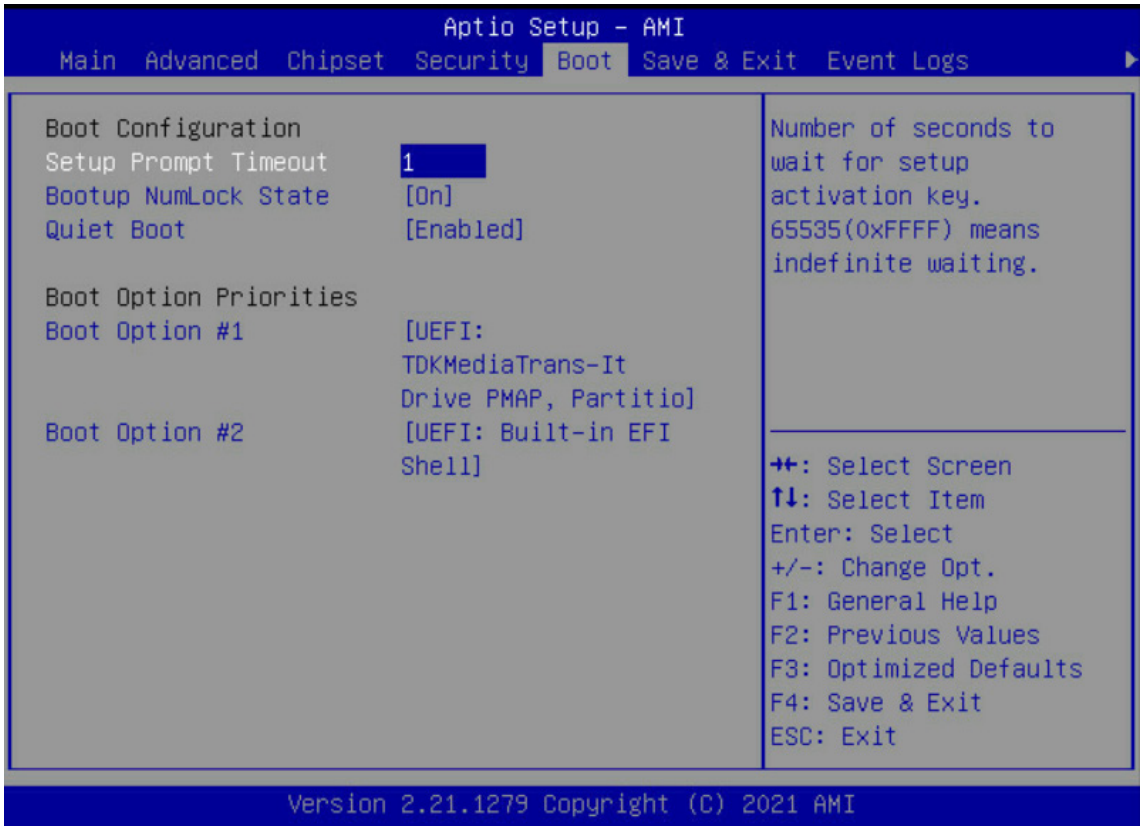
Chipset		
PCIe Link Training	1 step	2 step
PCIe Compliance Mode	On	Off

4.6 Security



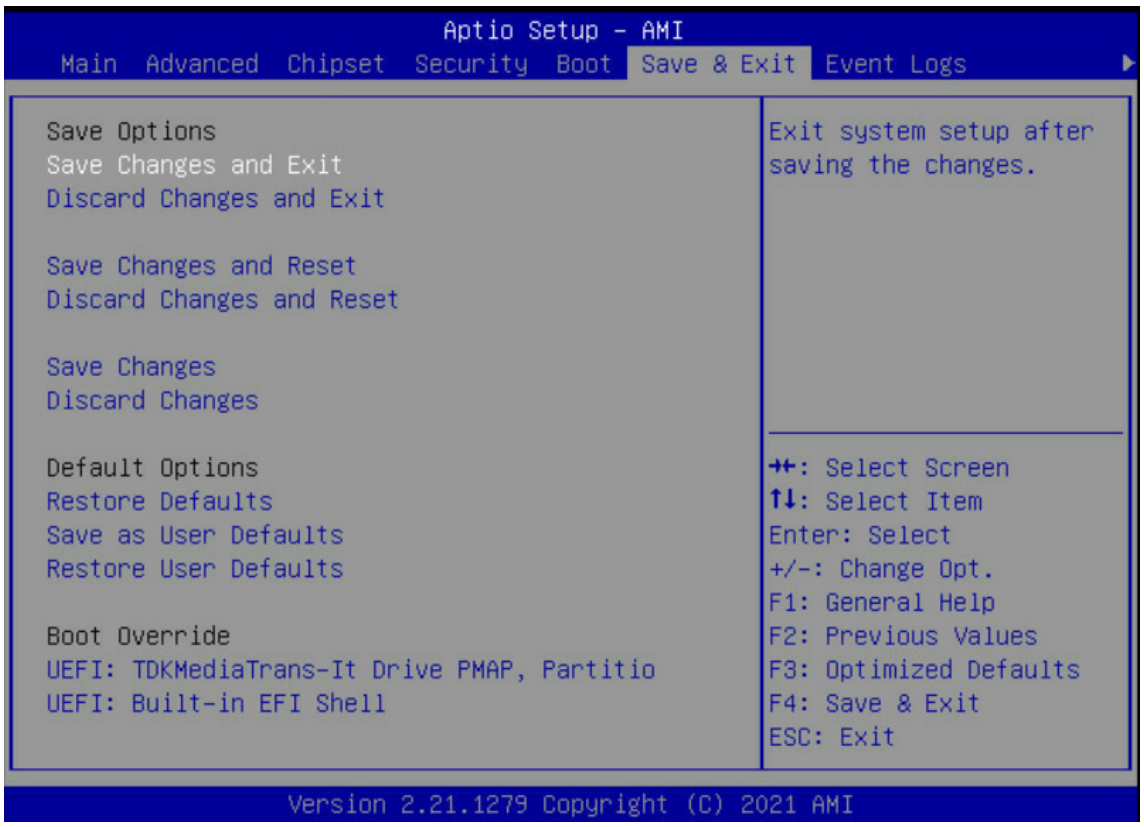
Security			
Administrator Password	Set administer password.		
Set User Password	Create new password.		
Secure Boot	Secure boot configuration.		
	Secure Boot	Enable	Disable
	Secure Boot Mode	Standard	Custom

4.7 Boot



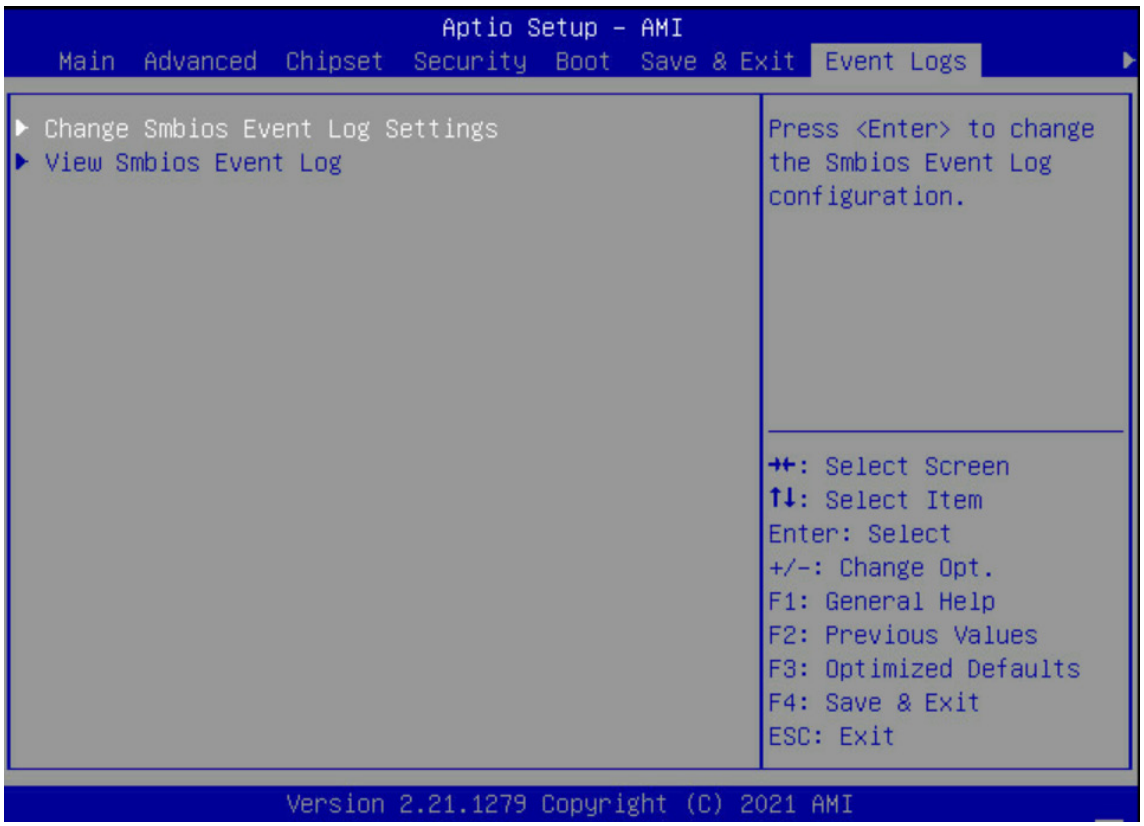
Boot		
Set Prompt Timeout	1	
Bootup Numlock State	On	Off
Quiet Boot	Enable	Disable
Boot Option #1/2	UEFI: Built-in EFI Shell	Disable
	UEFI: Built-in EFI Shell	Disable

4.8 Save and Exit



Save and Exit	
Save Change and Exit	Exits system setup after saving the changes.
Discard Changes and Exit	Exits system setup without saving any changes.
Save Changes and Reset	Resets the system after saving the changes.
Discard Changes and Reset	Resets system setup without saving any changes.
Save Changes	Saves changes done so far to any of the setup options.
Discard Changes	Discards changes done so far to any of the setup options
Restore Defaults	Restores/loads default values for all the setup options.
Save as User Defaults	Saves the changes done so far as user defaults.
Restore User Defaults	Restores the user defaults to all the setup options.

4.9 Event Logs

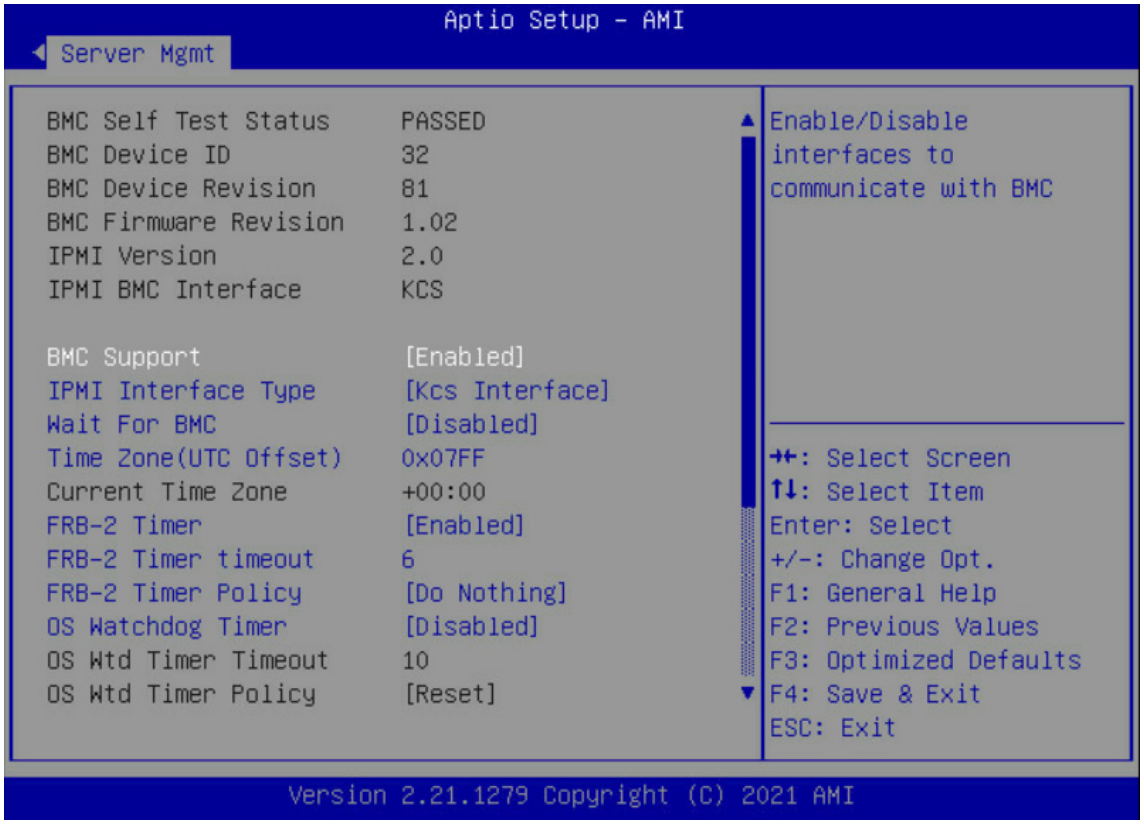


4.9.1 Change Smbios Event Log Settings

Configures Smbios event log.

Event Logs			
Smbios Event Log	Enable	Disable	
Erase Event Log	Yes, Next reset	Yes, Every reset	No
When Log is Full	Erase Immediately	Do Nothing	
Log System Boot Event	Enable	Disable	
MECI	1		
METW	60		
Log EFI Status Code	Enable	Disable	
Convert EFI Status Codes to Standard Smbios Type	Enable	Disable	

4.10 Server Mangement



Server Management							
BMC Support	Enable				Disable		
IPMI Interface Type	Kcs Interface				Bt Interface		
Wait for BMC	Enable				Disable		
Time Zone (UTC Offset)	0x07FF						
FRB-2 Timer	Enable				Disable		
FRB-2 Timer timeout	6		1-30				
FRB-2 Timer Policy	Do nothing	Reset			Power Down	Power Cycle	
OS Watchdog Timer	Enable				Disable		
Serial Mux	Enable				Disable		
System Event Log	SEL Components	Enable			Disable		
	Erase SEL	Yes, On next reset			Yes, On every reset	No	
	When SEL is Full	Erase Immediately			Delete Oldest Record	Do nothing	
	Log EFI Status Codes	Error code	Progress code		Both	Disable	
Bmc self test log	Erase Log	Yes, On every reset			No		
	When log is full	Clear Log			Do not log any more		
	Configuration Address source	Unspecified	Static		Dynamic BMC DHCP	Dynamic BMC Non DHCP	
BMC User Settings	Add User	Adds a user.					
	Delete User	Deletes a user.					
	Change User Settings	Changes user settings.					

4.11 BIOS Update Process

This is the manual for updating BIOS on Auriga system. Here are the update procedures:

For Shell:
1. Please run flash.nsh in BIOS folder.

For Linux:
1. Execute the below command
   ./flash.sh

NOTE
If you want to update bios from ROME to Milan, please contact AIC FAE.

NOTE
Please refer to "**Auriga_update_process.doc**" in BIOS release zip file for details.

4.12 BIOS Post Code

EPYC ROME

There are two ways to get post code,

1. Check the LED debug card
2. Execute the IPMI command as below

(1) Read the first 256 bytes:$ipmitool -I lanplus -H "$BMC_IP" -U "$BMC_USER" -P "$BMC_PASSWD" raw 0x32 0x73 0x00
(2) Read the next 256 bytes: $ipmitool -I lanplus -H "$BMC_IP" -U "$BMC_USER" -P "$BMC_PASSWD" raw 0x32 0x73 0x02

e.g. $ipmitool -I lanplus -H 192.168.0.3 -U admin -P admin raw 0x32 0x73 0x00

NOTE
BMC IP: -H $BMC_IP
User Account: -U $BMC_USER
Password: -P $BMC_PASSWD

AMD PSP FW POST code (FW output 2 bytes post code,but user only can see low byte on LED card or IPMI command)

Post Code	Description
Memory test points	
0xE001	Memory structure initialization (Public interface)
0xE002	SPD Data processing (Public interface)
0xE003	Memory configuration (Public interface) Phase 1
0xE004	DRAM initialization
0xE005	ProcMemSPDChecking
0xE006	ProcMemModeChecking
0xE007	Speed and TCL configuration
0xE008	ProcMemSpdTiming
0xE009	ProcMemDramMapping
0xE00A	ProcMemPlatformSpecificConfig
0xE00B	ProcMemPhyCompensation
0xE00C	ProcMemStartDcts
0xE00D	ProcMemBeforeDramInit (Public interface)
0xE00E	ProcMemPhyFenceTraining
0xE00F	ProcMemSynchronizeDcts
0xE010	ProcMemSystemMemoryMapping
0xE011	ProcMemMtrrConfiguration
0xE012	ProcMemDramTraining
0xE013	ProcMemBeforeAnyTraining(Public interface)
PMU Test Points	
0xE014	ABL Mem - PMU - Before PMU Firmware load
0xE015	ABL Mem - PMU - After PMU Firmware load
0xE016	ABL Mem - PMU Populate SRAM Timing
0xE017	ABL Mem - PMU Populate SRAM Config
0xE018	ABL Mem - PMU Write SRAM Msg Block
0xE019	ABL Mem - Wait for Phy Cal Complete
0xE01A	ABL Mem - Phy Cal Complete
0xE01B	ABL Mem - PMU Start

0xE01C	ABL Mem - PMU Started
0xE01D	ABL Mem - PMU Waiting for Complete
0xE01E	ABL Mem - PMU Stage Dec Init
0xE01F	ABL Mem - PMU Stage Training Wr Lvl
0xE020	ABL Mem - PMU Stage Training Rx En
0xE021	ABL Mem - PMU Stage Training Rd Dqs
0xE022	ABL Mem - PMU Stage Traning Rd 2D
0xE023	ABL Mem - PMU Stage Training Wr 2D
0xE024	ABL Mem - PMU Queue Empty
0xE025	ABL Mem - PMU US message Start
0xE026	ABL Mem - PMU US message End
0xE027	ABL Mem - PMU Complete
0xE028	ABL Mem - PMU - After PMU Training
0xE029	ABL Mem - PMU - Before Disable PMU
Original Post code	
0xE02A	ABL Mem - ProcMemTransmitDqsTraining
0xE02B	ABL Mem - Start write sweep
0xE02C	ABL Mem - Set Transmit DQ delay
0xE02D	ABL Mem - Write test pattern
0xE02E	ABL Mem - Read Test pattern
0xE02F	ABL Mem - Compare Test pattern
0xE030	ABL Mem - Update results
0xE031	ABL Mem - Start Find passing window
0xE032	ABL Mem - ProcMemMaxRdLatencyTraining
0xE033	ABL Mem - Start sweep
0xE034	ABL Mem - Set delay
0xE035	ABL Mem - Write test pattern
0xE036	ABL Mem - Read Test pattern
0xE037	ABL Mem - Compare Test pattern
0xE038	ABL Mem - Online Spare init
0xE039	ABL Mem - Chip select Interleave Init
0xE03A	ABL Mem - Node Interleave Init
0xE03B	ABL Mem - Channel Interleave Init
0xE03C	ABL Mem - ECC initialization
0xE03D	ABL Mem - Platform Specific Init
0xE03E	ABL Mem - Before callout for "AgesaReadSpd"
0xE03F	ABL Mem - After callout for "AgesaReadSpd"
0xE040	ABL Mem - Before optional callout "AgesaHookBeforeDramInit"
0xE041	ABL Mem - After optional callout "AgesaHookBeforeDramInit"
0xE042	ABL Mem - Before optional callout "AgesaHookBeforeDQSTraining"
0xE043	ABL Mem - After optional callout "AgesaHookBeforeDQSTraining"
0xE044	ABL Mem - Before optional callout "AgesaHookBeforeDramInit"
0xE045	ABL Mem - After optional callout "AgesaHookBeforeDramInit"
0xE046	ABL Mem - After MemDataInit
0xE047	ABL Mem - Before InitializeMCT
0xE048	ABL Mem - Before LV DDR3
0xE049	ABL Mem - Before InitMCT

0xE04A	ABL Mem - Before OtherTiming
0xE04B	ABL Mem - Before UMAMemTyping
0xE04C	ABL Mem - Before SetDqsEccTmgs
0xE04D	ABL Mem - Before MemClr
0xE04E	ABL Mem - Before On DIMM Thermal
0xE04F	ABL Mem - Before DMI
0xE050	ABL MEM - End of phase 3 memory code
CPU test points	
0xE051	Entry point CPU init after training
0xE052	Exit point CPU init after training
0xE053	Entry point CPU APOB data init
0xE054	Exit point CPU APOB data init
0xE055	Entry point CPU Optimized boot init
0xE056	Exit point CPU Optimized boot init
0xE057	Entry point CPU APOB EDC info init
0xE058	Exit point CPU APOB EDC info init
0xE059	Entry point CPU APOB CCD map data init
0xE05A	Exit point CPU APOB CCD map data init
Extended memory test point	
0xE080	ProcMemSendMRS2
0xE081	Sedding MRS3
0xE082	Sending MRS1
0xE083	Sending MRS0
0xE084	Continuous Pattern Read
0xE085	Continuous Pattern Write
0xE086	Mem: 2d RdDqs Training begin
0xE087	Mem: Before optional callout to platform BIOS to change External Vref during 2d Training
0xE088	Mem: After optional callout to platform BIOS to change External Vref during 2d Training
0xE089	Configure DCT For General use begin
0xE08A	Configure DCT For training begin
0xE08B	Configure DCT For Non-Explicit
0xE08C	Configure to Sync channels
0xE08D	Allocate C6 Storage
0xE08E	Before LV DDR4
0xE08F	Before LV DDR3
Gnb Earlier init	
0xE090	TP0x90
0xE091	GNB earlier interface
0xE092	GNB internal debug code
0xE093	GNB internal debug code
0xE094	GNB internal debug code
0xE095	GNB internal debug code
0xE096	GNB internal debug code
0xE097	GNB internal debug code
0xE098	GNB internal debug code
0xE099	GNB internal debug code

0xE09A	GNB internal debug code
0xE09B	GNB internal debug code
0xE09C	GNB internal debug code
0xE09D	GNB internal debug code
0xE09E	GNB internal debug code
0xE09F	GNB internal debug code
0xE0A0	TP0xA0
0xE0A1	GNB internal debug code
0xE0A2	GNB internal debug code
0xE0A3	GNB internal debug code
0xE0A4	GNB internal debug code
0xE0A5	GNB internal debug code
0xE0A6	GNB internal debug code
0xE0A7	GNB internal debug code
0xE0A8	GNB internal debug code
0xE0A9	GNB internal debug code
0xE0AA	GNB internal debug code
0xE0AB	GNB internal debug code
0xE0AC	GNB internal debug code
0xE0AD	GNB internal debug code
0xE0AE	GNB internal debug code
0xE0AF	GNB internal debug code
0xE0B0	Abl1Begin
0xE0B1	ABL 1 Initialization
0xE0B2	ABL 1 DF Early
0xE0B3	ABL 1 DF Pre Training
0xE0B4	ABL 1 Debug Synchronization
0xE0B5	ABL 1 Error Detected
0xE0B6	ABL 1 Global memory error detected
0xE0B7	ABL 1 End
0xE0B8	ABL 2 Begin
0xE0B9	ABL 2 Initialization
0xE0BA	ABL 2 After Training
0xE0BB	ABL 2 Debug Synchronization
0xE0BC	ABL 2 Error detected
0xE0BD	ABL 2 Global memory error detected
0xE0BE	ABL 2 End
0xE0BF	ABL 3 Begin
0xE0C0	ABL 3 Initialziation
0xE1C0	ABL 3 GMI/xGMI Initialization Stage 1
0xB1C0	ABL 3 GMI/xGMI Initialization Stage 1 Warning
0xF1C0	ABL 3 GMI/xGMI Initialization Stage 2 Error
0xE2C0	ABL 3 GMI/xGMI Initialization Stage 2
0xB2C0	ABL 3 GMI/xGMI Initialization Stage 2 Warning
0xF2C0	ABL 3 GMI/xGMI Initialization Stage 2 Error
0xE3C0	ABL 3 GMI/xGMI Initialization Stage 3
0xB3C0	ABL 3 GMI/xGMI Initialization Stage 3 Warning
0xF3C0	ABL 3 GMI/xGMI Initialization Stage 3 Error

0xE4C0	ABL 3 GMI/xGMI Initialization Stage 4
0xB4C0	ABL 3 GMI/xGMI Initialization Stage 4 Warning
0xF4C0	ABL 3 GMI/xGMI Initialization Stage 4 Error
0xE5C0	ABL 3 GMI/xGMI Initialization Stage 5
0xB5C0	ABL 3 GMI/xGMI Initialization Stage 5 Warning
0xF5C0	ABL 3 GMI/xGMI Initialization Stage 5 Error
0xE6C0	ABL 3 GMI/xGMI Initialization Stage 6
0xB6C0	ABL 3 GMI/xGMI Initialization Stage 6 Warning
0xF6C0	ABL 3 GMI/xGMI Initialization Stage 6 Error
0xE7C0	ABL 3 GMI/xGMI Initialization Stage 7
0xE8C0	ABL 3 GMI/xGMI Initialization Stage 8
0xE9C0	ABL 3 GMI/xGMI Initialization Stage 9
0xF9C0	ABL 3 GMI/xGMI Initialization Stage 9 Error
0xEAC0	ABL 3 GMI/xGMI Initialization Stage 10
0xFAC0	ABL 3 GMI/xGMI Initialization Stage 10 Error
0xE0C1	Abl3ProgramUmcKeys
0xE0C2	ABL 3 DF Finial Initalization
0xE0C3	ABL 3 Execute Synchronization Function
0xE0C4	ABL 3 Debug Synchronization Function
0xE0C5	ABL 3 Error Detected
0xE0C6	ABL 3 Global memroy error detected
0xE0C7	ABL 4 Initialiation - cold boot
0xE0C8	ABL 4 Memory test - cold boot
0xE0C9	ABL 4 APOB Initialzation - cold boot
0xE0CA	ABL 4 Finalize memory settings - cold boot
0xE0CB	ABL 4 CPU Initialize Optimized Boot - cold boot
0xE0CC	ABL 4 Gmi Pcie Training - cold boot
0xE0CD	ABL 4 Cold boot End
0xE0CE	ABL 4 Initialization - Resume boot
0xE0CF	ABL 4 Resume End
0xE0D0	ABL 4 End Cold/Resume boot
0xE0D1	ABL 2 memory initialization
0xE0D2	ABL 3 memory initialization
0xE0D3	ABL 3 End
0xE0D4	ABL 1 Enter Memory Flow
0xE0D5	Memorry flow memory clock synchronization
0xE0E0	Before IDS calls out to get IDS data
0xE0E1	After IDS calls out to get IDS data
PMU test points	
0xE0F9	Failed PMU training.
0xE0FA	End of phase 1 memory code
0xE0FB	End of phase 2 memory code
ABL0 test points	
0xE0FC	Abl0Begin
0xE0FD	ABL 0 End
0xE0FE	Abl0 Begin with Fatal Mode
0xE0FF	ABL 0 End with Fatal Mode

ABL5 test points	
0xE100	ABL 7 End
0xE101	ABL 7 Resume boot
0xE102	ABL 6 End
0xE103	ABL 6 Initialization
0xE104	End of phase 1b memory code
0xE105	ABL 1b memory initialization
0xE106	ABL 6 Global memroy error detected
0xE107	ABL 1b Debug Synchronization Function
0xE108	ABL 4b Debug Synchronization Function
0xE109	AblbBegin
0xE10A	Ab4bBegin
0xE10B	BSP encountered HMAC fail on APOB Header
0xE10C	ABL 18 End
0xE10D	ABL 18 Resume boot
0xE2A0	ABL Eroor General ASSERT
0xE2A1	Unknown Error
0xE2A3	ABL Error Log Inig Error
0xE2A4	ABL Error for On DIMM thermal Heap allocation error
0xE2A5	ABL Error for memory test error
0xE2A6	ABL Error while executing memory test error
0xE2A7	ABL Error DDR Post Packge Repair Mem Auto Heap Alloc error
0xE2A8	ABL Error for DDR Post Package repair Apob Heap Alloc error
0xE2A9	ABL Error for DDR Post Package Repair No PPR Table Heap Aloc error
0xE2AA	ABL Error for Ecc Mem Auto Aloc Error error
0xE2AB	ABL Error for Soc Scan Heap Aloc error
0xE2AC	ABL Error for Soc Scan No Die error
0xE2AD	ABL Error for Nb Tech Heap Aloc error
0xE2AE	ABL Error for No Nb Constructor error
0xE2B0	ABL Error for No Tech Constructor error
0xE2B1	ABL Error for ABL1b Auto Alocation error
0xE2B2	ABL Error for ABL1b No NB Constructor error
0xE2B3	ABL Error for ABL2 No Nb Constructor error
0xE2B4	ABL Error for ABL3 Auto Allocation error
0xE2B5	ABL Error for ABL3 No Nb Constructor error
0xE2B6	ABL Error for ABL1b General error
0xE2B7	ABL Error for ABL2 General error
0xE2B8	ABL Error for ABL3 General error
0xE2B9	ABL Error for Get Target Speed error
0xE2BA	ABL Error for Flow P1 Family Support error
0xE2BB	ABL Error for No Valid Ddr4 Dimms error
0xE2BC	ABL Error for No Dimm Present error
0xE2BD	ABL Error for Flow P2 Family Supprot error
0xE2BE	ABL Error for Heap Deallocation for PMU Sram Msg Block error
0xE2BF	ABL Error for DDR Recovery error
0xEBC0	ABL Error for RRW Test error
0xE2C1	ABL Error for On Die Thermal error
0xE2C2	ABL Error for Heap Allocation For Dct Struct Amd Ch Def structure error

0xE2C3	ABL Error for Heap Allocation for PMU SRAM Msg block error
0xE2C4	ABL Error for Heap Phy PLL lock Flure error
0xE2C5	ABL Error for Pmu Training error
0xE2C6	ABL Error for Failure to Load or Verify PMU FW error
0xE2C7	ABL Error for Allocate for PMU SRAM Msg Block No Init error
0xE2C8	ABL Error for Failure BIOS PMU FW Mismatch AGESA PMU FW version error
0xE2C9	ABL Error for Agesa memory test error
0xE2CA	ABL Error for Deallocate for PMU SRAM Msg Block error
0xE2CB	ABL Error for Module Type Mismatch RDIMM error
0xE2CC	ABL Error for Module type Mismatch LRDIMM error
0xE2CD	ABL Error for MEm Auto NVDIM error
0xE2CE	ABL Error for Unknowm Responce error
0xE2CF	ABL Error for Over Clock Error RRW Test Results Error
0xE2D0	ABL Error for Over Clock Error PMU Training Error
0xE2D1	ABL Error for ABL1 General Error
0xE2D2	ABL Error for ABL2 General Error
0xE2D3	ABL Error for ABL3 General Error
0xE2D4	ABL Error for ABL4 General Error
0xE2D5	ABL Error over clock Mem Init Error
0xE2D6	ABL Error over clock Mem Other Error
0xE2D7	ABL Error for ABL6 General Error
0xE2D8	ABL Error Event Log Error
0xE2D9	ABL Error FATAL ABL1 Log Error
0xE2DA	ABL Error FATAL ABL2 Log Error
0xE2DB	ABL Error FATAL ABL3 Log Error
0xE2DC	ABL Error FATAL ABL4 Log Error
0xE2DD	ABL Error Slave Sync function execution Error
0xE2DE	ABL Error Slave Sync communicaton with data set to master Error
0xE2DF	ABL Error Slave broadcast communication from master to slave Error
0xE2E0	ABL Error FATAL ABL6 Log Error
0xE2E1	ABL Error Slave Offline Error
0xE2E2	ABL Error Slave Informs Master Error Info Error
0xE2E3	ABL Error Error Heap Locate for PMU SRAM Msg Block Error
0xE2E4	ABL Error ABL2 Auto Error
0xE2E5	ABL Error Flow P3 Family support Error
0xE2E5	ABL Error Abl 4 Gen Error
0xE2EB	ABL Error MBIST Heap Allocation Error
0xE2EC	ABL Error MBIST Results Error
0xE2ED	ABL Error NO Dimm Smcus Info Error
0xE2EE	ABL Error Por Max Freq Table Error
0xE2EF	ABL Error Unsupproted DIMM Config Error
0xE2F0	ABL Error No Ps Table Error
0xE2F1	ABL Error Cad Bus Timing Not Found Error
0xE2F2	ABL Error Data Bus Timing Not Found Error
0xE2F3	ABL Error LrDIMM IBT Not Found Error
0xE2F4	ABL Error Unsupprote Dimm Config Max Freq Error Error
0xE2F5	ABL Error Mr0 Not Found Error

0xE2F6	ABL Error Obt Pattern Not found Error
0xE2F7	ABL Error Rc10 Op Speed Not FOund Error
0xE2F8	ABL Error Rc2 Ibt Not Found Error
0xE2F9	ABL Error Rtt Not Found Error
0xE2FA	ABL Error Checksum ReStrt Results Error
0xE2FB	ABL Error No Chipselect Results Error
0xE2FC	ABL Error No Common Cas Latency Results Error
0xE2FD	ABL Error Cas Latecncy exceeds Taa Max Error
0xE2FE	ABL Error Nvdimm Arm Missmatch Power Policy Error
0xE2FF	ABL Error Nvdimm Arm Missmatch Power Source Error
0xE300	ABL Error ABL 1 Mem Init Error
0xE301	ABL Error ABL 2 Mem Init Error
0xE302	ABL Error ABL 4 Mem Init Error
0xE303	ABL Error ABL 6 Mem Init Error
0xE304	ABL Error ABL 1 error repor Error
0xE305	ABL Error ABL 2 error repor Error
0xE306	ABL Error ABL 3 error repor Error
0xE307	ABL Error ABL 4 error repor Error
0xE308	ABL Error ABL 6 error repor Error
0xE30A	ABL Error message slave sync function execution Error
0xE30B	ABL Error slave offline Error
0xE30C	ABL Error Sync Master Error
0xE30D	ABL Error Slave Informs Master Info Message Error
0xE30E	ABL Error Mix Hynix LRDIMM with other vendor LRDIMM in a channel
0xE30F	ABL Error General Assert Error
0xE310	ABL ErrorNo Dimms On Any Channel in sysem
0xE311	ABL Error for Shared Heap Aloc error
0xE312	ABL Error for Main Heap Aloc error
0xE313	ABL Error for Shared Heap loc error
0xE314	ABL Error for Main Heap loc error
0xE316	ABL Error No memory available in system
0xE320	ABL Error Mixed Ecc and Non-Ecc DIMM in a channel
0xE321	ABL Error Mixed 3DS and Non-3DS DIMM in a channel
0xE322	ABL Error Mixed x4 and x8 DIMM in a channel

Insyde POST Code

Post Code	Description
0x01	CPU power on and switch to Protected mode
0x02	Patching CPU microcode
0x03	Setup Cache as RAM
0x04	PCIE MMIO Base Address initial
0x05	CPU Generic MSR initial
0x06	Setup CPU speed
0x07	Cache as RAM test
0x08	Tune CPU frequency ratio to maximum level
0x09	Setup BIOS ROM cache
0x0A	Enter Boot Firmware Volume
0x70	Super I/O initial

0x71	CPU Early Initial
0x72	Multi-processor Early initial
0x73	HyperTransport initial
0x74	PCIE MMIO BAR Initial
0x75	North Bridge Early Initial
0x76	South Bridge Early Initial
0x77	PCIE Training
0x78	TPM Initial
0x79	SMBUS Early Initial
0x7A	Clock Generator Initial
0x7B	Internal Graphic device early initial, PEI_IGDOpRegion
0x7C	HECI Initial
0x7D	Watchdog timer initial
0x7E	Memory Initial for Normal boot.
0x7F	Memory Initial for Crisis Recovery
0x80	Simple Memory test
0x81	TXT function early initial
0x82	Start to use Memory
0x83	Set cache for physical memory
0x84	Recovery device initial
0x85	Found Recovery image
0x86	Recovery image not found
0x87	Load Recovery Image complete
0x88	Start Flash BIOS with Recovery image
0x89	Loading BIOS image to RAM
0x8A	Loading DXE core
0x8B	Enter DXE core
0x8C	iFFS Transition Start
0x8D	iFFS Transition End
0x40	TPM initial in DXE
0x41	South bridge SPI initial
0x42	Setup Reset service, DXE_CF9Reset
0x43	South bridge Serial GPIO initial, DXE_SB_SerialGPIO_INIT
0x44	Setup SMM ACCESS service
0x45	North bridge Middle initial
0x46	Super I/O DXE initial
0x47	Setup Legacy Region service, DXE_LegacyRegion
0x48	South Bridge Middle Initial
0x49	Identify Flash device
0x4A	Fault Tolerant Write verification
0x4B	Variable Service Initial
0x4C	Fail to initial Variable Service
0x4D	MTC Initial
0x4E	CPU Middle Initial
0x4F	Multi-processor Middle Initial
0x50	SMBUS Driver Initial
0x51	8259 Initial
0x52	RTC Initial

0x53	SATA Controller early initial
0x54	Setup SMM Control service, DXE_SMMControler_INIT
0x55	Setup Legacy Interruput service, DXE_LegacyInterrupt
0x56	Relocate SMM BASE
0x57	SMI test
0x58	VTD Initial
0x59	Legacy BIOS initial
0x5A	Legacy interrupt function initial
0x5B	ACPI Table Initial
0x5C	Setup SB SMM Dispatcher service, DXE_SB_Dispatch
0x5D	Setup SB IOTRAP Service
0x5E	Build AMT Table
0x5F	PPM Initial
0x60	HECIDRV Initial
0x61	Variable store garbage collection and reclaim operation
0x62	Do not support flash part (which is defined in SpiDevice.c)
0x10	Enter BDS entry
0x11	Install Hotkey service
0x12	ASF Initial
0x13	PCI enumeration
0x14	PCI resource assign complete
0x15	PCI enumeration complete
0x16	Keyboard Controller, Keyboard and Moust initial
0x17	Video device initial
0x18	Error report device initial
0x19	USB host controller initial
0x1A	USB BUS driver initial
0x1B	USB device driver initial
0x1C	Console device initial fail
0x1D	Display logo or system information
0x1E	IDE controller initial
0x1F	SATA controller initial
0x20	SIO controller initial
0x21	ISA BUS driver initial
0x22	Floppy device initial
0x23	Serial device initial
0x24	IDE device initial
0x25	AHCI device initial
0x26	Dispatch option ROMs
0x27	Get boot device information
0x28	End of boot selection
0x29	Enter Setup Menu
0x2A	Enter Boot manager
0x2B	Try to boot system to OS
0x2C	Shadow Misc Option ROM
0x2D	Save S3 resume required data in RAM
0x2E	Last Chipset initial before boot to OS
0x2F	Start to boot Legacy OS

0x30	Start to boot UEFI OS
0x31	Prepare to Boot to Legacy OS
0x32	Send END of POST Message to ME via HECI
0x33	Last Chipset initial before boot to Legacy OS.
0x34	Ready to Boot Legacy OS.
0x35	Fast recovery start flash
0x36	SDHC device initial
0x37	Ata Legacy device initial
0x38	SD Legacy device initial
0xF9	No Boot Device, PostBDS_NO_BOOT_DEVICE
0xFB	UEFI Boot Start Image, PostBDS_START_IMAGE
0xFD	Legacy 16 boot entry
0xFE	Try to Boot with INT 19
0xA0	Identify Flash device in SMM
0xA2	SMM service initial
0xA6	OS call ACPI enable function
0xA7	ACPI enable function complete
0xA4	Enter S4
0xA5	Enter S5
0xA8	OS call ACPI disable function
0xA9	ACPI disable function complete
0x54	Prepare to enter S4
0x55	Prepare to enter S5
0xE4	System wakeup from S4
0xE5	System wakeup from S5

EPYC Milan

There are two ways to get post code,

1. Check the LED debug card
2. Execute the IPMI command as below

(1) Read the first 256 bytes:$ipmitool -I lanplus -H "$BMC_IP" -U "$BMC_USER" -P "$BMC_PASSWD" raw 0x32 0x73 0x00
(2) Read the next 256 bytes: $ipmitool -I lanplus -H "$BMC_IP" -U "$BMC_USER" -P "$BMC_PASSWD" raw 0x32 0x73 0x02

e.g. $ipmitool -I lanplus -H 192.168.0.3 -U admin -P admin raw 0x32 0x73 0x00

NOTE
BMC IP: -H $BMC_IP
User Account: -U $BMC_USER
Password: -P $BMC_PASSWD

AMD PSP FW POST code (FW output 2 bytes post code,but user only can see low byte on LED card or IPMI command)

Post Code	Description
Memory test points	
0xE001	Memory structure initialization (Public interface)
0xE002	SPD Data processing (Public interface)
0xE003	Memory configuration (Public interface) Phase 1
0xE004	DRAM initialization
0xE005	ProcMemSPDChecking
0xE006	ProcMemModeChecking
0xE007	Speed and TCL configuration
0xE008	ProcMemSpdTiming
0xE009	ProcMemDramMapping
0xE00A	ProcMemPlatformSpecificConfig
0xE00B	ProcMemPhyCompensation
0xE00C	ProcMemStartDcts
0xE00D	ProcMemBeforeDramInit (Public interface)
0xE00E	ProcMemPhyFenceTraining
0xE00F	ProcMemSynchronizeDcts
0xE010	ProcMemSystemMemoryMapping
0xE011	ProcMemMtrrConfiguration
0xE012	ProcMemDramTraining
0xE013	ProcMemBeforeAnyTraining(Public interface)
PMU Test Points	
0xE014	ABL Mem - PMU - Before PMU Firmware load
0xE015	ABL Mem - PMU - After PMU Firmware load
0xE016	ABL Mem - PMU Populate SRAM Timing
0xE017	ABL Mem - PMU Populate SRAM Config
0xE018	ABL Mem - PMU Write SRAM Msg Block
0xE019	ABL Mem - Wait for Phy Cal Complete
0xE01A	ABL Mem - Phy Cal Complete
0xE01B	ABL Mem - PMU Start

0xE01C	ABL Mem - PMU Started
0xE01D	ABL Mem - PMU Waiting for Complete
0xE01E	ABL Mem - PMU Stage Dec Init
0xE01F	ABL Mem - PMU Stage Training Wr Lvl
0xE020	ABL Mem - PMU Stage Training Rx En
0xE021	ABL Mem - PMU Stage Training Rd Dqs
0xE022	ABL Mem - PMU Stage Traning Rd 2D
0xE023	ABL Mem - PMU Stage Training Wr 2D
0xE024	ABL Mem - PMU Queue Empty
0xE025	ABL Mem - PMU US message Start
0xE026	ABL Mem - PMU US message End
0xE027	ABL Mem - PMU Complete
0xE028	ABL Mem - PMU - After PMU Training
0xE029	ABL Mem - PMU - Before Disable PMU
Original Post code	
0xE02A	ABL Mem - ProcMemTransmitDqsTraining
0xE02B	ABL Mem - Start write sweep
0xE02C	ABL Mem - Set Transmit DQ delay
0xE02D	ABL Mem - Write test pattern
0xE02E	ABL Mem - Read Test pattern
0xE02F	ABL Mem - Compare Test pattern
0xE030	ABL Mem - Update results
0xE031	ABL Mem - Start Find passing window
0xE032	ABL Mem - ProcMemMaxRdLatencyTraining
0xE033	ABL Mem - Start sweep
0xE034	ABL Mem - Set delay
0xE035	ABL Mem - Write test pattern
0xE036	ABL Mem - Read Test pattern
0xE037	ABL Mem - Compare Test pattern
0xE038	ABL Mem - Online Spare init
0xE039	ABL Mem - Chip select Interleave Init
0xE03A	ABL Mem - Node Interleave Init
0xE03B	ABL Mem - Channel Interleave Init
0xE03C	ABL Mem - ECC initialization
0xE03D	ABL Mem - Platform Specific Init
0xE03E	ABL Mem - Before callout for "AgesaReadSpd"
0xE03F	ABL Mem - After callout for "AgesaReadSpd"
0xE040	ABL Mem - Before optional callout "AgesaHookBeforeDramInit"
0xE041	ABL Mem - After optional callout "AgesaHookBeforeDramInit"
0xE042	ABL Mem - Before optional callout "AgesaHookBeforeDQSTraining"
0xE043	ABL Mem - After optional callout "AgesaHookBeforeDQSTraining"
0xE044	ABL Mem - Before optional callout "AgesaHookBeforeDramInit"
0xE045	ABL Mem - After optional callout "AgesaHookBeforeDramInit"
0xE046	ABL Mem - After MemDataInit
0xE047	ABL Mem - Before InitializeMCT
0xE048	ABL Mem - Before LV DDR3
0xE049	ABL Mem - Before InitMCT

0xE04A	ABL Mem - Before OtherTiming
0xE04B	ABL Mem - Before UMAMemTyping
0xE04C	ABL Mem - Before SetDqsEccTmgs
0xE04D	ABL Mem - Before MemClr
0xE04E	ABL Mem - Before On DIMM Thermal
0xE04F	ABL Mem - Before DMI
0xE050	ABL MEM - End of phase 3 memory code
CPU test points	
0xE051	Entry point CPU init after training
0xE052	Exit point CPU init after training
0xE053	Entry point CPU APOB data init
0xE054	Exit point CPU APOB data init
0xE055	Entry point CPU Optimized boot init
0xE056	Exit point CPU Optimized boot init
0xE057	Entry point CPU APOB EDC info init
0xE058	Exit point CPU APOB EDC info init
0xE059	Entry point CPU APOB CCD map data init
0xE05A	Exit point CPU APOB CCD map data init
Extended memory test point	
0xE080	ProcMemSendMRS2
0xE081	Sedding MRS3
0xE082	Sending MRS1
0xE083	Sending MRS0
0xE084	Continuous Pattern Read
0xE085	Continuous Pattern Write
0xE086	Mem: 2d RdDqs Training begin
0xE087	Mem: Before optional callout to platform BIOS to change External Vref during 2d Training
0xE088	Mem: After optional callout to platform BIOS to change External Vref during 2d Training
0xE089	Configure DCT For General use begin
0xE08A	Configure DCT For training begin
0xE08B	Configure DCT For Non-Explicit
0xE08C	Configure to Sync channels
0xE08D	Allocate C6 Storage
0xE08E	Before LV DDR4
0xE08F	Before LV DDR3
Gnb Earlier init	
0xE090	TP0x90
0xE091	GNB earlier interface
0xE092	GNB internal debug code
0xE093	GNB internal debug code
0xE094	GNB internal debug code
0xE095	GNB internal debug code
0xE096	GNB internal debug code
0xE097	GNB internal debug code
0xE098	GNB internal debug code
0xE099	GNB internal debug code

0xE09A	GNB internal debug code
0xE09B	GNB internal debug code
0xE09C	GNB internal debug code
0xE09D	GNB internal debug code
0xE09E	GNB internal debug code
0xE09F	GNB internal debug code
0xE0A0	TP0xA0
0xE0A1	GNB internal debug code
0xE0A2	GNB internal debug code
0xE0A3	GNB internal debug code
0xE0A4	GNB internal debug code
0xE0A5	GNB internal debug code
0xE0A6	GNB internal debug code
0xE0A7	GNB internal debug code
0xE0A8	GNB internal debug code
0xE0A9	GNB internal debug code
0xE0AA	GNB internal debug code
0xE0AB	GNB internal debug code
0xE0AC	GNB internal debug code
0xE0AD	GNB internal debug code
0xE0AE	GNB internal debug code
0xE0AF	GNB internal debug code
0xE0B0	Abl1Begin
0xE0B1	ABL 1 Initialization
0xE0B2	ABL 1 DF Early
0xE0B3	ABL 1 DF Pre Training
0xE0B4	ABL 1 Debug Synchronization
0xE0B5	ABL 1 Error Detected
0xE0B6	ABL 1 Global memory error detected
0xE0B7	ABL 1 End
0xE0B8	ABL 2 Begin
0xE0B9	ABL 2 Initialization
0xE0BA	ABL 2 After Training
0xE0BB	ABL 2 Debug Synchronization
0xE0BC	ABL 2 Error detected
0xE0BD	ABL 2 Global memory error detected
0xE0BE	ABL 2 End
0xE0BF	ABL 3 Begin
0xE0C0	ABL 3 Initialziation
0xE1C0	ABL 3 GMI/xGMI Initialization Stage 1
0xB1C0	ABL 3 GMI/xGMI Initialization Stage 1 Warning
0xF1C0	ABL 3 GMI/xGMI Initialization Stage 2 Error
0xE2C0	ABL 3 GMI/xGMI Initialization Stage 2
0xB2C0	ABL 3 GMI/xGMI Initialization Stage 2 Warning
0xF2C0	ABL 3 GMI/xGMI Initialization Stage 2 Error
0xE3C0	ABL 3 GMI/xGMI Initialization Stage 3
0xB3C0	ABL 3 GMI/xGMI Initialization Stage 3 Warning
0xF3C0	ABL 3 GMI/xGMI Initialization Stage 3 Error

0xE4C0	ABL 3 GMI/xGMI Initialization Stage 4
0xB4C0	ABL 3 GMI/xGMI Initialization Stage 4 Warning
0xF4C0	ABL 3 GMI/xGMI Initialization Stage 4 Error
0xE5C0	ABL 3 GMI/xGMI Initialization Stage 5
0xB5C0	ABL 3 GMI/xGMI Initialization Stage 5 Warning
0xF5C0	ABL 3 GMI/xGMI Initialization Stage 5 Error
0xE6C0	ABL 3 GMI/xGMI Initialization Stage 6
0xB6C0	ABL 3 GMI/xGMI Initialization Stage 6 Warning
0xF6C0	ABL 3 GMI/xGMI Initialization Stage 6 Error
0xE7C0	ABL 3 GMI/xGMI Initialization Stage 7
0xE8C0	ABL 3 GMI/xGMI Initialization Stage 8
0xE9C0	ABL 3 GMI/xGMI Initialization Stage 9
0xF9C0	ABL 3 GMI/xGMI Initialization Stage 9 Error
0xEAC0	ABL 3 GMI/xGMI Initialization Stage 10
0xFAC0	ABL 3 GMI/xGMI Initialization Stage 10 Error
0xE0C1	Abl3ProgramUmcKeys
0xE0C2	ABL 3 DF Finial Initalization
0xE0C3	ABL 3 Execute Synchronization Function
0xE0C4	ABL 3 Debug Synchronization Function
0xE0C5	ABL 3 Error Detected
0xE0C6	ABL 3 Global memroy error detected
0xE0C7	ABL 4 Initialiation - cold boot
0xE0C8	ABL 4 Memory test - cold boot
0xE0C9	ABL 4 APOB Initialzation - cold boot
0xE0CA	ABL 4 Finalize memory settings - cold boot
0xE0CB	ABL 4 CPU Initialize Optimized Boot - cold boot
0xE0CC	ABL 4 Gmi Pcie Training - cold boot
0xE0CD	ABL 4 Cold boot End
0xE0CE	ABL 4 Initialization - Resume boot
0xE0CF	ABL 4 Resume End
0xE0D0	ABL 4 End Cold/Resume boot
0xE0D1	ABL 2 memory initialization
0xE0D2	ABL 3 memory initialization
0xE0D3	ABL 3 End
0xE0D4	ABL 1 Enter Memory Flow
0xE0D5	Memorry flow memory clock synchronization
0xE0E0	Before IDS calls out to get IDS data
0xE0E1	After IDS calls out to get IDS data
PMU test points	
0xE0F9	Failed PMU training.
0xE0FA	End of phase 1 memory code
0xE0FB	End of phase 2 memory code
ABL0 test points	
0xE0FC	Abl0Begin
0xE0FD	ABL 0 End
0xE0FE	Abl0 Begin with Fatal Mode
0xE0FF	ABL 0 End with Fatal Mode

ABL5 test points	
0xE100	ABL 7 End
0xE101	ABL 7 Resume boot
0xE102	ABL 6 End
0xE103	ABL 6 Initialization
0xE104	End of phase 1b memory code
0xE105	ABL 1b memory initialization
0xE106	ABL 6 Global memroy error detected
0xE107	ABL 1b Debug Synchronization Function
0xE108	ABL 4b Debug Synchronization Function
0xE109	AblbBegin
0xE10A	Ab4bBegin
0xE10B	BSP encountered HMAC fail on APOB Header
0xE10C	ABL 18 End
0xE10D	ABL 18 Resume boot
0xE10E	ABL 15 End
0xE10F	ABL 15 Initialization
0xE110	Before UMC based device initialization
0xE111	After UMC based device initialization
0xE2A0	ABL Eroor General ASSERT
0xE2A1	Unknown Error
0xE2A3	ABL Error Log Inig Error
0xE2A4	ABL Error for On DIMM thermal Heap allocation error
0xE2A5	ABL Error for memory test error
0xE2A6	ABL Error while executing memory test error
0xE2A7	ABL Error DDR Post Packge Repair Mem Auto Heap Alloc error
0xE2A8	ABL Error for DDR Post Package repair Apob Heap Alloc error
0xE2A9	ABL Error for DDR Post Package Repair No PPR Table Heap Aloc error
0xE2AA	ABL Error for Ecc Mem Auto Aloc Error error
0xE2AB	ABL Error for Soc Scan Heap Aloc error
0xE2AC	ABL Error for Soc Scan No Die error
0xE2AD	ABL Error for Nb Tech Heap Aloc error
0xE2AE	ABL Error for No Nb Constructor error
0xE2B0	ABL Error for No Tech Constructor error
0xE2B1	ABL Error for ABL1b Auto Alocation error
0xE2B2	ABL Error for ABL1b No NB Constructor error
0xE2B3	ABL Error for ABL2 No Nb Constructor error
0xE2B4	ABL Error for ABL3 Auto Allocation error
0xE2B5	ABL Error for ABL3 No Nb Constructor error
0xE2B6	ABL Error for ABL1b General error
0xE2B7	ABL Error for ABL2 General error
0xE2B8	ABL Error for ABL3 General error
0xE2B9	ABL Error for Get Target Speed error
0xE2BA	ABL Error for Flow P1 Family Support error
0xE2BB	ABL Error for No Valid Ddr4 Dimms error
0xE2BC	ABL Error for No Dimm Present error
0xE2BD	ABL Error for Flow P2 Family Supprot error
0xE2BE	ABL Error for Heap Deallocation for PMU Sram Msg Block error

0xE2BF	ABL Error for DDR Recovery error
0xEBC0	ABL Error for RRW Test error
0xE2C1	ABL Error for On Die Thermal error
0xE2C2	ABL Error for Heap Allocation For Dct Struct Amd Ch Def structure error
0xE2C3	ABL Error for Heap Allocation for PMU SRAM Msg block error
0xE2C4	ABL Error for Heap Phy PLL lock Flure error
0xE2C5	ABL Error for Pmu Training error
0xE2C6	ABL Error for Failure to Load or Verify PMU FW error
0xE2C7	ABL Error for Allocate for PMU SRAM Msg Block No Init error
0xE2C8	ABL Error for Failure BIOS PMU FW Mismatch AGESA PMU FW version error
0xE2C9	ABL Error for Agesa memory test error
0xE2CA	ABL Error for Deallocate for PMU SRAM Msg Block error
0xE2CB	ABL Error for Module Type Mismatch RDIMM error
0xE2CC	ABL Error for Module type Mismatch LRDIMM error
0xE2CD	ABL Error for MEm Auto NVDIM error
0xE2CE	ABL Error for Unknowm Responce error
0xE2CF	ABL Error for Over Clock Error RRW Test Results Error
0xE2D0	ABL Error for Over Clock Error PMU Training Error
0xE2D1	ABL Error for ABL1 General Error
0xE2D2	ABL Error for ABL2 General Error
0xE2D3	ABL Error for ABL3 General Error
0xE2D4	ABL Error for ABL4 General Error
0xE2D5	ABL Error over clock Mem Init Error
0xE2D6	ABL Error over clock Mem Other Error
0xE2D7	ABL Error for ABL6 General Error
0xE2D8	ABL Error Event Log Error
0xE2D9	ABL Error FATAL ABL1 Log Error
0xE2DA	ABL Error FATAL ABL2 Log Error
0xE2DB	ABL Error FATAL ABL3 Log Error
0xE2DC	ABL Error FATAL ABL4 Log Error
0xE2DD	ABL Error Slave Sync function execution Error
0xE2DE	ABL Error Slave Sync communicaton with data set to master Error
0xE2DF	ABL Error Slave broadcast communication from master to slave Error
0xE2E0	ABL Error FATAL ABL6 Log Error
0xE2E1	ABL Error Slave Offline Error
0xE2E2	ABL Error Slave Informs Master Error Info Error
0xE2E3	ABL Error Error Heap Locate for PMU SRAM Msg Block Error
0xE2E4	ABL Error ABL2 Auto Error
0xE2E5	ABL Error Flow P3 Family support Error
0xE2E5	ABL Error Abl 4 Gen Error
0xE2EB	ABL Error MBIST Heap Allocation Error
0xE2EC	ABL Error MBIST Results Error
0xE2ED	ABL Error NO Dimm Smcus Info Error
0xE2EE	ABL Error Por Max Freq Table Error
0xE2EF	ABL Error Unsupproted DIMM Config Error
0xE2F0	ABL Error No Ps Table Error

0xE2F1	ABL Error Cad Bus Timing Not Found Error
0xE2F2	ABL Error Data Bus Timing Not Found Error
0xE2F3	ABL Error LrDIMM IBT Not Found Error
0xE2F4	ABL Error Unsupprote Dimm Config Max Freq Error Error
0xE2F5	ABL Error Mr0 Not Found Error
0xE2F6	ABL Error Obt Pattern Not found Error
0xE2F7	ABL Error Rc10 Op Speed Not FOund Error
0xE2F8	ABL Error Rc2 Ibt Not Found Error
0xE2F9	ABL Error Rtt Not Found Error
0xE2FA	ABL Error Checksum ReStrt Results Error
0xE2FB	ABL Error No Chipselect Results Error
0xE2FC	ABL Error No Common Cas Latency Results Error
0xE2FD	ABL Error Cas Latecncy exceeds Taa Max Error
0xE2FE	ABL Error Nvdimm Arm Missmatch Power Policy Error
0xE2FF	ABL Error Nvdimm Arm Missmatch Power Source Error
0xE300	ABL Error ABL 1 Mem Init Error
0xE301	ABL Error ABL 2 Mem Init Error
0xE302	ABL Error ABL 4 Mem Init Error
0xE303	ABL Error ABL 6 Mem Init Error
0xE304	ABL Error ABL 1 error repor Error
0xE305	ABL Error ABL 2 error repor Error
0xE306	ABL Error ABL 3 error repor Error
0xE307	ABL Error ABL 4 error repor Error
0xE308	ABL Error ABL 6 error repor Error
0xE30A	ABL Error message slave sync function execution Error
0xE30B	ABL Error slave offline Error
0xE30C	ABL Error Sync Master Error
0xE30D	ABL Error Slave Informs Master Info Message Error
0xE30E	ABL Error Mix Hynix LRDIMM with other vendor LRDIMM in a channel
0xE30F	ABL Error General Assert Error
0xE310	ABL ErrorNo Dimms On Any Channel in sysem
0xE311	ABL Error for Shared Heap Aloc error
0xE312	ABL Error for Main Heap Aloc error
0xE313	ABL Error for Shared Heap loc error
0xE314	ABL Error for Main Heap loc error
0xE316	ABL Error No memory available in system
0xE320	ABL Error Mixed Ecc and Non-Ecc DIMM in a channel
0xE321	ABL Error Mixed 3DS and Non-3DS DIMM in a channel
0xE322	ABL Error Mixed x4 and x8 DIMM in a channel
0xE323	ABL Memory MBIST Rrw default test
0xE324	ABL Memory MBIST Interface test
0xE325	ABL Memory MBIST DataEye
0xE326	ABL Memory Post Package Repair
0xE327	ABL Error S0i3 DF restore buffer Error
0xE328	ABL Error CPU OPN Mismatch in case of Multi Socket population
0xE329	Recoverable APCB Checksum Error
0xE32A	Fatal APCB Checksum Error
0xE32B	ABL Error BIST Failure

0xE32C	ABL Memory Heal BIST Write
0xE32D	ABL Memory Heal BIST Read
0xE32E	ABL Error BIST Failure

AMD AGESA POST Code (FW output 2 bytes post code,but user only can see low byte on LED card or IPMI command)

Post Code	Description
Universal Post Code	
0xA001	Universal ACPI entry
0xA002	Universal ACPI exit
0xA003	Universal ACPI abort
0xA004	Universal SMBIOS entry
0xA005	Universal SMBIOS exit
0xA006	Universal SMBIOS abort
[0xA1XX] For CZ only memory Post codes	
0xA101	Memory structure initialization (Public interface)
0xA102	SPD Data processing (Public interface)
0xA103	Memory configuration (Public interface)
0xA104	DRAM initialization
0xA105	TpProcMemSPDChecking
0xA106	TpProcMemModeChecking
0xA107	Speed and TCL configuration
0xA108	TpProcMemSpdTiming
0xA109	TpProcMemDramMapping
0xA10A	TpProcMemPlatformSpecificConfig
0xA10B	TPProcMemPhyCompensation
0xA10C	TpProcMemStartDcts
0xA10D	(Public interface)
0xA10E	TpProcMemPhyFenceTraining
0xA10F	TpProcMemSynchronizeDcts
0xA110	TpProcMemSystemMemoryMapping
0xA111	TpProcMemMtrrConfiguration
0xA112	TpProcMemDramTraining
0xA113	(Public interface)
0xA114	TpProcMemWriteLevelizationTraining
0xA115	Below 800Mhz first pass start
0xA116	Above 800Mhz second pass start
0xA117	Target DIMM configured
0xA118	Prepare DIMMS for WL
0xA119	Configure DIMMS for WL
0xA11A	TpProcMemReceiverEnableTraining
0xA11B	Start sweep loop
0xA11C	Set receiver Delay
0xA11D	Write test pattern
0xA11E	Read test pattern
0xA11F	Compare test pattern
0xA120	Calculate MaxRdLatency per channel

0xA121	TpProcMemReceiveDqsTraining
0xA122	Set Write Data delay
0xA123	Write test pattern
0xA124	Start read sweep
0xA125	Set Receive DQS delay
0xA126	Read Test pattern
0xA127	Compare Test pattern
0xA128	Update results
0xA129	Start Find passing window
0xA12A	TpProcMemTransmitDqsTraining
0xA12B	Start write sweep
0xA12C	Set Transmit DQ delay
0xA12D	Write test pattern
0xA12E	Read Test pattern
0xA12F	Compare Test pattern
0xA130	Update results
0xA131	Start Find passing window
0xA132	TpProcMemMaxRdLatencyTraining
0xA133	Start sweep
0xA134	Set delay
0xA135	Write test pattern
0xA136	Read Test pattern
0xA137	Compare Test pattern
0xA138	Online Spare init
0xA139	Bank Interleave Init
0xA13A	Node Interleave Init
0xA13B	Channel Interleave Init
0xA13C	ECC initialization
0xA13D	Platform Specific Init
0xA13E	Before callout for "AgesaReadSpd"
0xA13F	After callout for "AgesaReadSpd"
0xA140	Before optional callout "AgesaHookBeforeDramInit"
0xA141	After optional callout "AgesaHookBeforeDramInit"
0xA142	Before optional callout "AgesaHookBeforeDQSTraining"
0xA143	After optional callout "AgesaHookBeforeDQSTraining"
0xA144	Before optional callout "AgesaHookBeforeDramInit"
0xA145	After optional callout "AgesaHookBeforeDramInit"
0xA146	After MemDataInit
0xA147	Before InitializeMCT
0xA148	Before LV DDR3
0xA149	Before InitMCT
0xA14A	Before OtherTiming
0xA14B	Before UMAMemTyping
0xA14C	Before SetDqsEccTmgs
0xA14D	Before MemClr
0xA14E	Before On DIMM Thermal
0xA14F	Before DMI
0xA150	End of memory code

0xA151	Entry point S3Init
0xA180	Sending MRS2
0xA181	Sedding MRS3
0xA182	Sending MRS1
0xA183	Sending MRS0
0xA184	Continuous Pattern Read
0xA185	Continuous Pattern Write
0xA186	Mem: 2d RdDqs Training begin
0xA187	Mem: Before optional callout to platform BIOS to change External Vref during 2d Training
0xA188	Mem: After optional callout to platform BIOS to change External Vref during 2d Training
0xA189	Configure DCT For General use begin
0xA18A	Configure DCT For training begin
0xA18B	Configure DCT For Non-Explicit
0xA18C	Configure to Sync channels
0xA18D	Allocate C6 Storage
0xA18E	Before LV DDR4
BR CPU	
0xA190	BR before AP launch
0xA191	Install AP launched PPI
0xA192	BR after AP launch
0xA193	Before CPU PM
0xA194	Enable IO Cstate
0xA195	Enable C6
0xA196	Install CCX PEI complete PPI
0xA197	BR CPU memory done call back entry
0xA198	Before APM weights
0xA199	After APM weights
0xA19A	BR CPU memory done call back end
0xA19B	BR Init Mid entry
0xA19C	BR enable APM
0xA19D	BR Init Mid install protocol
0xA19E	BR Init Mid end
0xA19F	BR Init Late entry
0xA1A0	BR Init Late install protocol
0xA1A1	BR Init Late end
0xA1A2	BR DXE install complete protocol
0xA1A3	UNB install complete PPI
0xA1A4	UNB AfterApLaunch callback entry
0xA1A5	UNB AfterApLaunch callback end
S3 Interface Post Code	
0xA1EC	Before the S3 save code calls out to allocate a buffer
0xA1ED	After the S3 save code calls out to allocate a buffer
0xA1EE	Before the memory S3 save code calls out to allocate a buffer
0xA1EF	After the memory S3 save code calls out to allocate a buffer
0xA1F0	Before the memory code calls out to locate a buffer
0xA1F1	After the memory code calls out to locate a buffer

0xA1F2	Before the memory code calls out to locate a buffer
0xA1F3	After the memory code calls out to locate a buffer
0xA1F4	Before the memory code calls out to locate a buffer
0xA1F5	After the memory code calls out to locate a buffer
0xA1F6	Before the memory code calls out to locate a buffer
0xA1F7	After the memory code calls out to locate a buffer
PMU Post Code	
0xA1F9	Failed PMU training.
PSP V1 Modules	
0xA501	PspPeiV1 entry
0xA502	PspPeiV1 exit
0xA503	MemoryDiscoveredPpiCallback entry
0xA504	MemoryDiscoveredPpiCallback exit
0xA507	PspDxeV1 entry
0xA508	PspDxeV1 exit
0xA50A	PspDxeV1 PspPciEnumerationCompleteCallBack entry
0xA50B	PspDxeV1 PspPciEnumerationCompleteCallBack exit
0xA50C	PspDxeV1 ready to boot entry
0xA50D	PspDxeV1 ready to boot exit
0xA50E	PspSmmV1 entry
0xA50F	PspSmmV1 exit
0xA510	PspSmmV1 SwSmiCallBack entry, build the S3 save area for resume
0xA511	PspSmmV1 SwSmiCallBack exit, build the S3 save area for resume
0xA512	PspSmmV1 BspSmmResumeVector entry
0xA513	PspSmmV1 BspSmmResumeVector exit
0xA514	PspSmmV1 ApSmmResumeVector entry
0xA515	PspSmmV1 ApSmmResumeVector exit
0xA516	PspP2CmboxV1 entry
0xA517	PspP2CmboxV1 exit
PSP V2 Modules	
0xA521	PspPeiV2 entry
0xA522	PspPeiV2 exit
0xA523	PspDxeV2 entry
0xA524	PspDxeV2 exit
0xA525	PspDxeV2 PspMpServiceCallBack entry
0xA526	PspDxeV2 PspMpServiceCallBack exit
0xA527	PspDxeV2 FlashAccCallBack entry
0xA528	PspDxeV2 FlashAccCallBack exit
0xA529	PspDxeV2 ready to boot entry
0xA52A	PspDxeV2 ready to boot exit
0xA52B	PspDxeV2 exit boot serivce entry
0xA52C	PspDxeV2 exit boot serivce exit
0xA52D	PspSmmV2 entry
0xA52E	PspSmmV2 exit
0xA52F	PspSmmV2 SwSmiCallBack entry, build the S3 save area for resume
0xA530	PspSmmV2 SwSmiCallBack exit, build the S3 save area for resume
0xA531	PspSmmV2 BspSmmResumeVector entry
0xA532	PspSmmV2 BspSmmResumeVector exit

0xA533	PspSmmV2 ApSmmResumeVector entry
0xA534	PspSmmV2 ApSmmResumeVector exit
0xA535	PspP2CmboxV2 entry
0xA536	PspP2CmboxV2 exit
0xA537	TpPspRecoverApcbFail
0xA539	PspDxeV2 ApcbAccCallBack entry
0xA53A	PspDxeV2 ApcbAccCallBack exit
PSP fTpm modules	
0xA540	PspfTpmPei entry
0xA541	PspfTpmPei exit
0xA542	PspfTpmPei memory callback entry
0xA543	PspfTpmPei memory callback exit
0xA544	PspfTpmDxe entry
0xA545	PspfTpmDxe exit
PSP dTpm modules	
0xA546	PspdTpmPei entry
0xA547	PspdTpmPei exit
HSP fTpm modules	
0xA548	HspfTpmPei entr
0xA549	HspfTpmPei exit
0xA54A	HspfTpmPei memory callback entry
0xA54B	HspfTpmPei memory callback exit
0xA54C	HspfTpmDxe entry
0xA54D	HspfTpmDxe exit
P2C mailbox Handling [0xA59X]	
0xA591	PspP2Cmbox Command SpiGetAttrib Handling entry
0xA592	PspP2Cmbox Command SpiSetAttrib Handling entry
0xA593	PspP2Cmbox Command SpiGetBlockSize Handling entry
0xA594	PspP2Cmbox Command SpiReadFV Handling entry
0xA595	PspP2Cmbox Command SpiWriteFV Handling entry
0xA596	PspP2Cmbox Command SpiEraseFV Handling entry
0xA597	PspP2Cmbox Command MboxPspCmdRpmcIncMc entry
0xA598	PspP2Cmbox Command TpMboxPspCmdRpmcReqMc entry
0xA599	PspP2Cmbox Command TpMboxPspCmdArsStatus entry
0xA59E	PspP2Cmbox Command Handling exit
0xA59F	PspP2Cmbox Command Handling Fail exit
C2P mailbox Handling [0xA601 ~ 0xA67F: before send C2P command, 0xA681 ~ 0xA6FF: wait C2P command]	
0xA600	PSP C2P mailbox entry base [0xA600 | Cmd]
0xA601	Before send C2P command MboxBiosCmdDramInfo
0xA602	Before send C2P command MboxBiosCmdSmmInfo
0xA603	Before send C2P command MboxBiosCmdSleep SxInfo
0xA604	Before send C2P command MboxBiosCmdRsmInfo
0xA605	Before send C2P command MboxBiosCmdQueryCap
0xA606	Before send C2P command MboxBiosCmdBootDone
0xA607	Before send C2P command MboxBiosCmdClearS3Sts
0xA608	Before send C2P command MboxBiosCmdS3DataInfo
0xA609	Before send C2P command MboxBiosCmdNop

0xA614	Before send C2P command MboxBiosCmdHSTIQuery
0xA617	Before send C2P command MboxBiosCmdClrSmmLock
0xA618	Before send C2P command MboxBiosCmdPcieInfo
0xA619	Before send C2P command MboxBiosCmdGetVersion
0xA61B	Before send C2P command MboxBiosCmdLockDFReg
0xA61D	Before send C2P command MboxBiosCmdSetApCsBase
0xA61E	Before send C2P command MboxBiosCmdKvmInfo
0xA61F	Before send C2P command MboxBiosCmdLockSpi
0xA620	Before send C2P command MboxBiosCmdScreenOnGpio
0xA621	Before send C2P command MboxBiosCmdSpiOpWhiteList
0xA622	Before send C2P command MboxBiosCmdRasEinj
0xA624	Before send C2P command MboxBiosCmdStartArs
0xA625	Before send C2P command MboxBiosCmdStopArs
0xA626	Before send C2P command MboxBiosCmdSetBootPartitionId
0xA627	Before send C2P command MboxBiosCmdPspCapsQuery
0xA628	Before send C2P command MboxBiosCmdArmorEnterSmmOnlyMode
0xA629	Before send C2P command MboxBiosCmdArmorEnforceWhitelist
0xA62A	Before send C2P command MboxBiosCmdArmorExecuteSpiCommand
0xA62B	Before send C2P command MboxBiosCmdArmorSwitchCsMode
0xA62C	Before send C2P command MboxBiosCmdDrtmInfoId
0xA62D	Before send C2P command MboxBiosCmdLaterSplFuse
0xA62F	Before send C2P command MboxBiosCmdValidateManOsSignature
0xA630	Before send C2P command MboxBiosCmdLockFCHReg
0xA639	Before send C2P command MboxBiosCmdSetRpmcAddress
0xA63F	Before send C2P command MboxBiosCmdSendIvrsAcpiTable
0xA640	Before send C2P command MboxBiosCmdTa
0xA642	Before send C2P command MboxBiosCmdQueryTCGLog
0xA680	PSP C2P mailbox exit base [0xA680 | Cmd]
0xA681	Wait C2P command MboxBiosCmdDramInfo finished
0xA682	Wait C2P command MboxBiosCmdSmmInfo finished
0xA683	Wait C2P command MboxBiosCmdSleep SxInfo finished
0xA684	Wait C2P command MboxBiosCmdRsmInfo finished
0xA685	Wait C2P command MboxBiosCmdQueryCap finished
0xA686	Wait C2P command MboxBiosCmdBootDone finished
0xA687	Wait C2P command MboxBiosCmdClearS3Sts finished
0xA688	Wait C2P command MboxBiosCmdS3DataInfo finished
0xA689	Wait C2P command MboxBiosCmdNop finished
0xA694	Wait C2P command MboxBiosCmdHSTIQuery finished
0xA697	Wait C2P command MboxBiosCmdClrSmmLock finished
0xA698	Wait C2P command MboxBiosCmdPcieInfo finished
0xA699	Wait C2P command MboxBiosCmdGetVersion finished
0xA69B	Wait C2P command MboxBiosCmdLockDFReg finished
0xA69D	Wait C2P command MboxBiosCmdSetApCsBase finished
0xA69E	Wait C2P command MboxBiosCmdKvmInfo finished
0xA69F	Wait C2P command MboxBiosCmdLockSpi finished
0xA6A0	Wait C2P command MboxBiosCmdScreenOnGpio finished
0xA6A1	Wait C2P command MboxBiosCmdSpiOpWhiteList finished

0xA6A2	Wait C2P command MboxBiosCmdRasEinj finished
0xA6A4	Wait C2P command MboxBiosCmdStartArs finished
0xA6A5	Wait C2P command MboxBiosCmdStopArs finished
0xA6A6	Wait C2P command MboxBiosCmdSetBootPartitionId finished
0xA6A7	Wait C2P command MboxBiosCmdPspCapsQuery finished
0xA6A8	Wait C2P command MboxBiosCmdArmorEnterSmmOnlyMode finished
0xA6A9	Wait C2P command MboxBiosCmdArmorEnforceWhitelist finished
0xA6AA	Wait C2P command MboxBiosCmdArmorExecuteSpiCommand finished
0xA6AB	Wait C2P command MboxBiosCmdArmorSwitchCsMode finished
0xA6AC	Wait C2P command MboxBiosCmdDrtmInfoId finished
0xA6AD	Wait C2P command MboxBiosCmdLaterSplFuse finished
0xA6AF	Wait C2P command MboxBiosCmdValidateManOsSignature finished
0xA6B0	Wait C2P command MboxBiosCmdLockFCHReg finished
0xA6B9	Wait C2P command MboxBiosCmdSetRpmcAddress finished
0xA6BF	Wait C2P command MboxBiosCmdSendIvrsAcpiTable finished
0xA6C0	Wait C2P command MboxBiosCmdTa finished
0xA6C2	Wait C2P command MboxBiosCmdQueryTCGLog finished
fTPM command Handling [0xA5FX]	
0xA5F0	PspfTpm send TPM command entry
0xA5F1	PspfTpm send TPM command exit
0xA5F2	PspfTpm receive TPM command entry
0xA5F3	PspfTpm receive TPM command exit
0xA5F4	HspfTpm send TPM command entry
0xA5F5	HspfTpm send TPM command exit
0xA5F6	HspfTpm receive TPM command entry
0xA5F7	HspfTpm receive TPM command exit
NbioBase	
0xA900	AmdNbioBase PEIM driver entry
0xA901	AmdNbioBase PEIM driver exit
0xA902	AmdNbioBase DXE driver entry
0xA903	AmdNbioBase DXE driver exit
PCIe	
0xA904	AmdNbioPcie PEIM driver entry
0xA905	AmdNbioPcie PEIM driver exit
0xA906	AmdNbioPcie DXE driver entry
0xA907	AmdNbioPcie DXE driver exit
GFX	
0xA908	AmdNbioGfx PEIM driver entry
0xA909	AmdNbioGfx PEIM driver exit0xA90A
0xA90A	AmdNbioGfx DXE driver entry
0xA90B	AmdNbioGfx DXE driver exit
IOMMU	
0xA90C	AmdNbioIommu DXE driver entry
0xA90D	AmdNbioIommu DXE driver exit
ALIB	
0xA90E	AmdNbioALIB DXE driver entry
0xA90F	AmdNbioALIB DXE driver exit

SMU	
0xA910	AmdSmuV8 PEIM driver entry
0xA911	AmdSmuV8 PEIM driver exit
0xA912	AmdSmuV8 DXE driver entry
0xA913	AmdSmuV8 DXE driver exit
0xA914	AmdSmuV9 PEIM driver entry
0xA915	AmdSmuV9 PEIM driver exit
0xA916	AmdSmuV9 DXE driver entry
0xA917	AmdSmuV9 DXE driver exit
0xA918	AmdSmuV10 PEIM driver entry
0xA919	AmdSmuV10 PEIM driver exit
0xA91A	AmdSmuV10 DXE driver entry
0xA91B	AmdSmuV10 DXE driver exit
0xA91C	AmdSmuV13 PEIM driver entry
0xA91D	AmdSmuV13 PEIM driver exit
0xA91E	AmdSmuV13 DXE driver entry
0xA91F	AmdSmuV13 DXE driver exit
IOMMU PEIM	
0xA920	AmdNbioIommu PEIM driver entry
0xA921	AmdNbioIommu PEIM driver exit
APCB DXE	
0xA922	APCB DXE Entry
0xA923	APCB DXE Exit
APCB SMM	
0xA924	APCB SMM Entry
0xA925	APCB SMM Exit
0xA930	Early Exit
0xA931	Early Exit
[0xA950, 0xA99F] NBIO PPI/PROTOCOL Callback	
0xA950	NbioTopologyConfigureCallback entry
0xA951	NbioTopologyConfigureCallback exit
0xA952	MemoryConfigDoneCallbackPpi entry
0xA953	MemoryConfigDoneCallbackPpi exit
0xA954	DxioInitializationCallbackPpi entry
0xA955	DxioInitializationCallbackPpi exit
0xA956	DispatchSmuV9Callback entry
0xA957	DispatchSmuV9Callback exit
0xA958	DispatchSmuV10Callback entry
0xA959	DispatchSmuV10Callback exit
0xA95A	AmdPcieMiscInit Event entry
0xA95B	AmdPcieMiscInit Event exit
0xA95C	NbioBaseHookReadyToBoot Event entry
0xA95D	NbioBaseHookReadyToBoot Event exit
0xA95E	NbioBaseHookPciIO Event entry
0xA95F	NbioBaseHookPciIO Event exit
0xA960	DispatchSmuV13Callback entry
0xA961	DispatchSmuV13Callback exit

[0xA980, 0xA99F] BR GNB task	
0xA970	GnbEarlyInterfaceCZ entry
0xA971	GnbEarlyInterfaceCZ exit
0xA972	PcieConfigurationInit entry
0xA973	PcieConfigurationInit exit
0xA974	GnbEarlierInterfaceCZ entry
0xA975	GnbEarlierInterfaceCZ exit
0xA976	PcieEarlyInterfaceCZ entry
0xA977	PcieEarlyInterfaceCZ exit
0xA978	PciePostEarlyInterfaceCZ entry
0xA979	PciePostEarlyInterfaceCZ exit
0xA97A	GfxConfigPostInterfaceCZ entry
0xA97B	GfxConfigPostInterfaceCZ exit
0xA97C	GfxPostInterfaceCZ entry
0xA97D	GfxPostInterfaceCZ exit
0xA97E	GnbPostInterfaceCZ entry
0xA97F	GnbPostInterfaceCZ exit
0xA980	PciePostInterfaceCZ entry
0xA981	PciePostInterfaceCZ exit
0xA982	GnbEnvInterfaceCZ entry
0xA983	GnbEnvInterfaceCZ exit
0xA984	GfxConfigEnvInterface entry
0xA985	GfxConfigEnvInterface exit
0xA986	GfxEnvInterfaceCZ entry
0xA987	GfxEnvInterfaceCZ exit
0xA988	GfxMidInterfaceCZ entry
0xA989	GfxMidInterfaceCZ exit
0xA98A	GfxIntInfoTableInterfaceCZ entry
0xA98B	GfxIntInfoTableInterfaceCZ exit
0xA98C	PcieMidInterfaceCZ entry
0xA98D	PcieMidInterfaceCZ exit
0xA98E	GnbMidInterfaceCZ entry
0xA98F	GnbMidInterfaceCZ exit
0xA990	GnbSmuMidInterfaceCZ entry
0xA991	GnbSmuMidInterfaceCZ exit
0xA992	InvokeAmdInitLate entry
0xA993	InvokeAmdInitLate exit
0xA994	GnbSmuServiceRequestV8 entry
0xA995	GnbSmuServiceRequestV8 exit
[0xACXX] assigned for AGESA CCX Module	
0xAC10	CCX IDS IDS_HOOK_CCX_AFTER_AP_LAUNCH
0xAC50	CCX PEI entry
0xAC51	CCX downcore entry
0xAC55	CCX DXE entry
0xAC56	CCX MP service callback entry
0xAC57	CCX Ready To Boot callback entry
0xAC58	CCX oc service callback entry
0xAC5D	CCX SMM entry

0xAC70	CCX PEI start to launch APs for S3
0xAC71	CCX PEI end of launching APs for S3
0xAC90	CCX start to launch AP
0xAC91	CCX launch AP is ended
0xAC92	CCX launch AP abort
0xAC93	CCX MP service abort
0xAC94	CCX cac weights
0xAC95	CCX before install CcxDone
0xAC96	CCX after install CcxDone
0xACE0	CCX PEI exit
0xACE1	CCX downcore exit
0xACE5	CCX DXE exit
0xACE6	CCX MP service callback exit
0xACE7	CCX Ready To Boot callback exit
0xACE8	CCX OC service callback exit
0xACED	CCX SMM exit
[0xADXX] assigned for AGESA DF Module	
0xAD50	DF PEI entry
0xAD55	DF DXE entry
0xAD56	DF Ready to Boot entry
0xAD57	DF NbioSmuServicesPpiCallback entry
0xAD58	DF NbioSmuServicesProtocolCallback entry
0xAD59	DF SMM entry
0xADE0	DF PEI exit
0xADE5	DF DXE exit
0xADE6	DF Ready to Boot exit
0xADE7	DF NbioSmuServicesPpiCallback exit
0xADE8	DF NbioSmuServicesProtocolCallback exit
0xADE9	DF SMM exit
@todo Remove unused FCH PCs	
0xAF01	FCH InitReset dispatch point
0xAF06	FCH InitEnv dispatch point
0xAF07	FCH InitMid dispatch point
0xAF08	FCH InitLate dispatch point
0xAF0B	FCH InitS3Early dispatch point
0xAF0C	FCH InitS3Late dispatch point
0xAF0D	FCH InitS3Early dispatch finished
0xAF0E	FCH InitS3Late dispatch finished
0xAF10	FCH Pei Entry
0xAF11	FCH Pei Exit
0xAF12	FCH MultiFch Pei Entry
0xAF13	FCH MultiFch Pei Exit
0xAF14	FCH Dxe Entry
0xAF15	FCH Dxe Exit
0xAF16	FCH MultiFch Dxe Entry
0xAF17	FCH MultiFch Dxe Exit
0xAF18	FCH Smm Entry
0xAF19	FCH Smm Exit

0xAF20	FCH Smm Dispatcher Entry
0xAF21	FCH Smm Dispatcher Exit
0xAF40	FCH InitReset HwAcpi
0xAF41	FCH InitReset AB Link
0xAF42	FCH InitReset LPC
0xAF43	FCH InitReset SPI
0xAF44	FCH InitReset eSPI
0xAF45	FCH InitReset SD
0xAF46	FCH InitReset eMMC
0xAF47	FCH InitReset SATA
0xAF48	FCH InitReset USB
0xAF49	FCH InitReset xGbE
0xAF4A	FCH InitReset USB Ready
0xAF4F	FCH InitReset HwAcpiP
0xAF50	FCH InitEnv HwAcpi
0xAF51	FCH InitEnv AB Link
0xAF52	FCH InitEnv LPC
0xAF53	FCH InitEnv SPI
0xAF54	FCH InitEnv eSPI
0xAF55	FCH InitEnv SD
0xAF56	FCH InitEnv eMMC
0xAF57	FCH InitEnv SATA
0xAF58	FCH InitEnv USB
0xAF59	FCH InitEnv xGbE
0xAF5F	FCH InitEnv HwAcpiP
0xAF60	FCH InitMid HwAcpi
0xAF61	FCH InitMid AB Link
0xAF62	FCH InitMid LPC
0xAF63	FCH InitMid SPI
0xAF64	FCH InitMid eSPI
0xAF65	FCH InitMid SD
0xAF66	FCH InitMid eMMC
0xAF67	FCH InitMid SATA
0xAF68	FCH InitMid USB
0xAF69	FCH InitMid xGbE
0xAF70	FCH InitLate HwAcpi
0xAF71	FCH InitLate AB Link
0xAF72	FCH InitLate LPC
0xAF73	FCH InitLate SPI
0xAF74	FCH InitLate eSPI
0xAF75	FCH InitLate SD
0xAF76	FCH InitLate eMMC
0xAF77	FCH InitLate SATA
0xAF78	FCH InitLate USB
0xAF79	FCH InitLate xGbE
0xAF7A	FCH PT load FW Entry
0xAF7B	FCH PT load FW Exit
0xAF7C	FCH PT_Plus load FW Entry

0xAF7D	FCH PT_Plus load FW Exit
0xAF80	FCH Device Enter D x Status 0xB000AFxx [4:0]:device ID; [6:5] 0:D0 3:D3; [7]==1 //PLAT-27512
0xAFB0	Bixby Pei Entry
0xAFB1	Bixby Pei Exit
0xAFB2	Bixby Dxe Entry
0xAFB3	Bixby Dxe Exit
0xAFB4	Bixby Smm Entry
0xAFB5	Bixby Smm Exit
0xAFB6	Bixby InitReset dispatch point
0xAFB7	Bixby InitMid dispatch point
0xAFB8	Bixby InitEnv dispatch point
0xAFB9	Bixby InitLate dispatch point
0xAFBA	Bixby InitS3Early dispatch point
0xAFBB	Bixby InitS3Late dispatch point
0xAFBC	Bixby InitS3Early dispatch finished
0xAFBD	Bixby InitS3Late dispatch finished
0xAFBE	Bixby InitReset SATA Entry
0xAFBF	Bixby InitReset SATA Exit
0xAFC0	Bixby InitMid SATA Entry
0xAFC1	Bixby InitMid SATA Exit
0xAFC2	Bixby InitEnv SATA Entry
0xAFC3	Bixby InitEnv SATA Exit
0xAFC4	Bixby InitLate SATA Entry
0xAFC5	Bixby InitLate SATA Exit
0xAFC6	Bixby InitReset USB Entry
0xAFC7	Bixby InitReset USB Exit
0xAFC8	Bixby InitMid USB Entry
0xAFC9	Bixby InitMid USB Exit
0xAFCA	Bixby InitEnv USB Entry
0xAFCB	Bixby InitEnv USB Exit
0xAFCC	Bixby InitLate USB Entry
0xAFCD	Bixby InitLate USB Exit
0xAFCE	Bixby InitEnv HwAcpiP
0xAFCF	Bixby InitReset HwAcpiP
0xAFFF	End of TP range for FCH

AMI POST Code

Post Code	Description
0x10	PEI core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization is started (CPU module specific)
0x13	Pre-memory CPU initialization is started (CPU module specific)
0x14	Pre-memory CPU initialization is started (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-memory North Bridge initialization is started (North Bridge module specific)
0x17	Pre-memory North Bridge initialization is started (North Bridge module specific)
0x18	Pre-memory North Bridge initialization is started (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization is started (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization is started (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization is started (South Bridge module specific)
0x1D~ 0x2A	Oem pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect(SPD) data reading
0x2C	Memory initialization. Meory Presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization. (Other)
0x30	Reserved for ASL (See ASL status codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. BootStrap Processor(BSP) initialization
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-memory North Bridge initialization is started
0x38	Post-memory North Bridge initialization is started (North Bridge module specific)
0x39	Post-memory North Bridge initialization is started (North Bridge module specific)
0x3A	Post-memory North Bridge initialization is started (North Bridge module specific)
0x3B	Post-memory South Bridge initialization is started
0x3C	Post-memory South Bridge initialization is started (South Bridge module specific)
0x3D	Post-memory South Bridge initialization is started (South Bridge module specific)

0x3E	Post-memory South Bridge initialization is started (South Bridge module specific)
0x3F~0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
S3 resume progress codes	
0xE0	S3 Resume is started (S3 Resume PPI is called by th DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4~0xE7	Reserved for future AMI progress codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loadded
0xF5~0xF7	Reserved for future AMI progress codes
DXE Phase	
0x60	DXE code is started
0x61	NVRAM initialization
0x62	Initialization of the South Bridge runtimes services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Brodge module specific)
0x6C	North Bridge DXE initialization (North Brodge module specific)
0x6D	North Bridge DXE initialization (North Brodge module specific)
0x6E	North Bridge DXE initialization (North Brodge module specific)
0x6F	North Bridge DXE initialization (North Brodge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	North Bridge DXE initialization (South Brodge module specific)
0x74	North Bridge DXE initialization (South Brodge module specific)
0x75	North Bridge DXE initialization (South Brodge module specific)
0x76	North Bridge DXE initialization (South Brodge module specific)
0x77	North Bridge DXE initialization (South Brodge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A~0x7F	Reserved for future AMI DXE codes
0x80~0x8F	OEM DXE initialization codes
0x90	Boot Device Selection(BDS) phase is started
0x91	Driver connecting is started

0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E~0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Satrt of Setup
0xAA	Reserved for ASL(See ASL Status Codes selection below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL(See ASL Status Codes selection below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM initialization
0xB3	System Reset
0xB4	USB Hot Plug
0xB5	PCI bus Hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reste (reset of NVRAM settings)
0xB8~0xBF	Reserved for future AMI codes
0xC0~0xCF	OEM BDS initialization codes
ACPI ASL Checkpoints	
0x01	System is entering S1 sleeping state
0x02	System is entering S2 sleeping state
0x03	System is entering S3 sleeping state
0x04	System is entering S4 sleeping state
0x05	System is entering S5 sleeping state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state

0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

Chapter 5. BMC Configuration Settings

This chapter displays the configuration settings of IPMI BMC in your system device.

5.1 Login

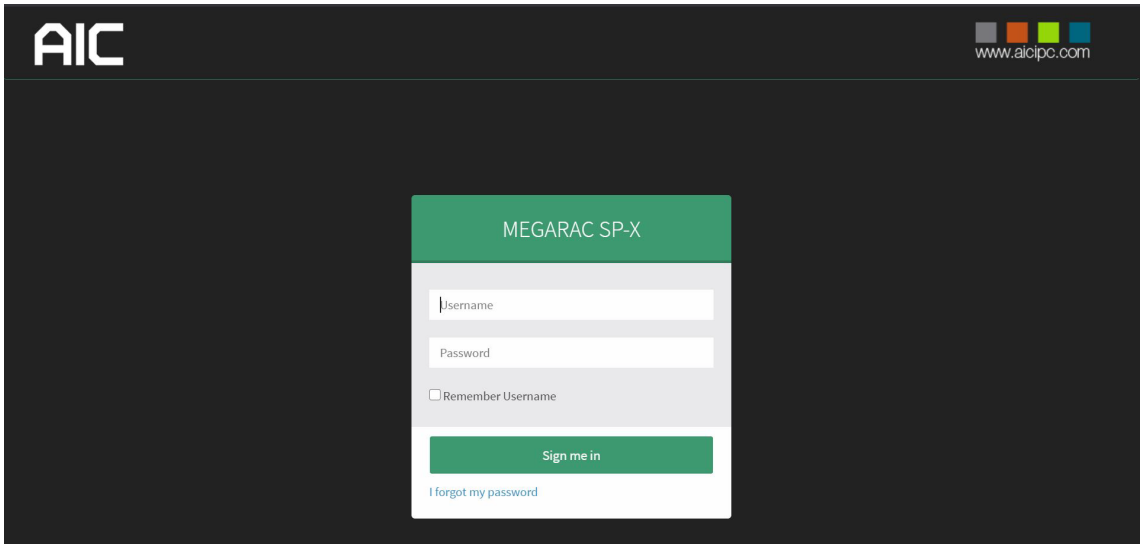
NOTE
This feature works with the html5. Please use a browser that supports html5.

The IP address below is an example using the default IP setting. The IP address is configurable.

Step 1 Open the browser and then type in the default BMC IP address: 172.200.20.199.

Step 2 Use the default user name and password for first-time BMC WEB GUI login. Users need to set authorization before sending a command.
Change the tab to **Authorization**.

Type:	Default
Account:	admin
Password:	admin



NOTE
-The default user name and password are in lower-case characters.
-Users who login with the root user name and password will have full administrative power. The root password can be changed after login.

5.2 Web GUI

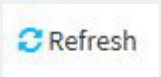
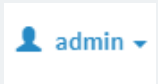
5.2.1 Menu Bar

Click to select the options of the menu bar.

Menu	Description
Dashboard	The Dashboard page gives the overall information about the status of a device.
Sensor	The Sensor Readings page displays all the sensor related information.
FRU Information	The FRU Information page displays the details for FRU devices in the system.
Logs & Reports	The Logs and Reports page monitors and reports on the status of IPMI event and video.
Settings	The Settings page allows you to configure various basic settings, such as date & time, KMV Mouse, Services, and etc.
Remote Control	The Remote Control page allows you to remotely manage server hardware components.
Image Redirection	The Image Redirection page is used to configure the image into BMC for redirection.
Power Control	The Power Control page allows you to view and control the power of your server.
Maintenance	This group of pages allows you to do maintenance tasks on the device.
Sign out	The Sign out page allows you to log out of the web GUI.

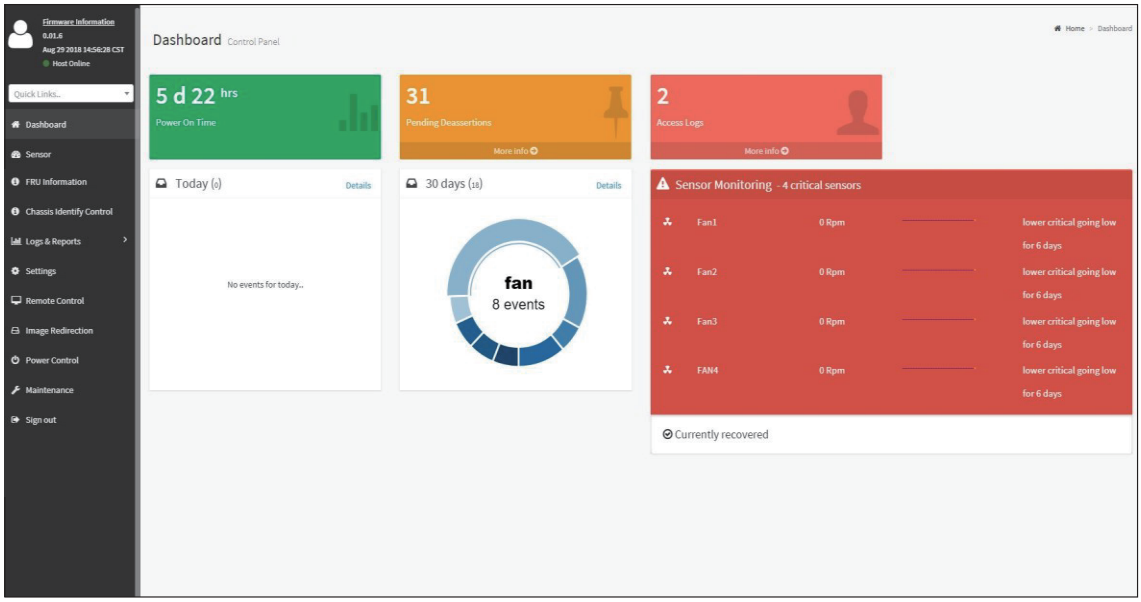
5.2.2 User Information and Quick Button

The user information and quick access buttons are located at the top right corner. It displays the logged-in user, his/her privilege and the four quick buttons allowing you to perform different functions.

Button		Description
User		Only valid commands are allowed.
Operator		All BMC commands are allowed except for the configuration commands that can change the behavior of the out-of-hand interfaces.
Administrator		All BMC commands are allowed.
No access		Login access denied.
	Notification	Click to view notification messages.
	Warning	Click to view warning messages.
	Sync	Click to synchronize with the latest sensor and event log updates.
	Refresh	Click to reload the current page.
	User-inform	**Sign out**: Click to log out of the GUI **Profile:** Click to enter the User Management Configuration dialog box in figure xx.
	Help	Click to view more details on field descriptions.

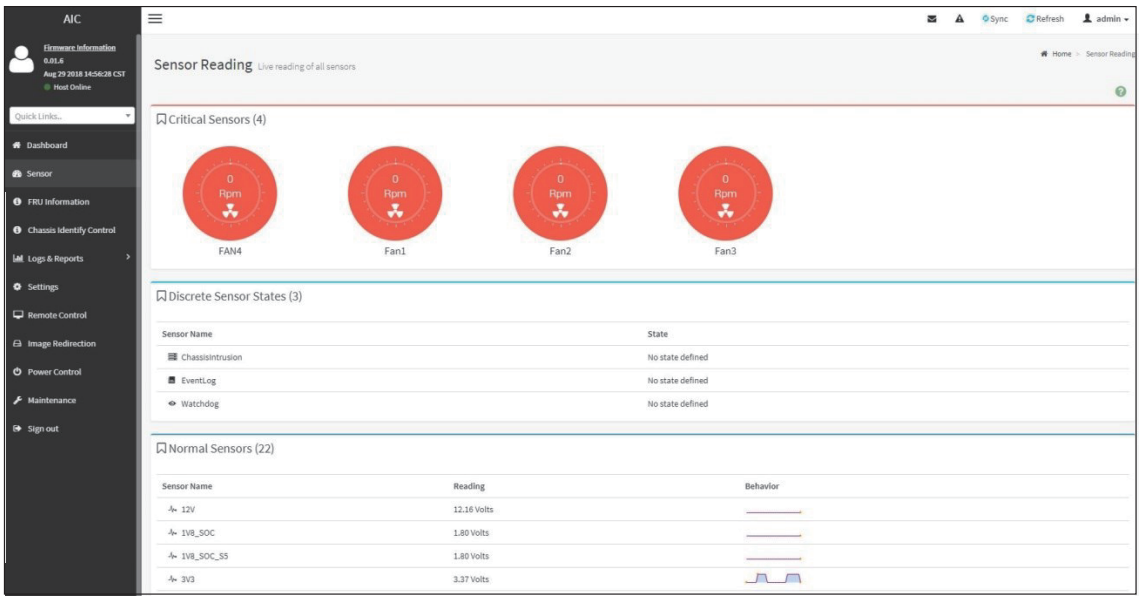
5.2.3 Dashboard

The Dashboard page displays device, system information, and assert logs.
Click **Dashboard** on the menu bar to view the overall information of the server.



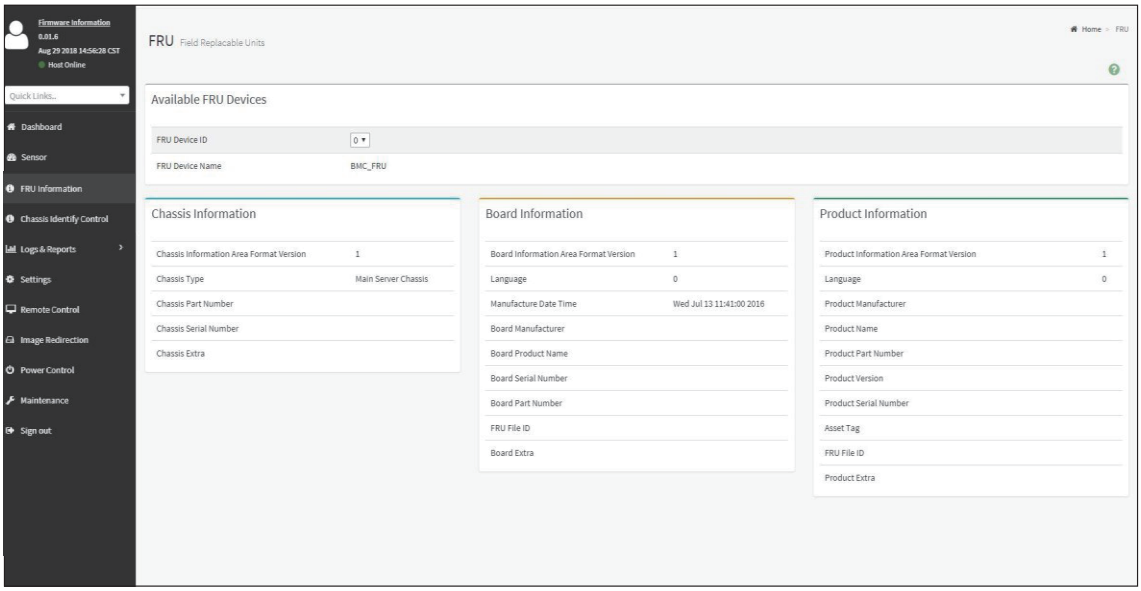
5.2.4 Sensor

The Sensor page displays the status and records on related sensors. Click a record to view detailed information on a particular sensor.



5.2.5 FRU Information

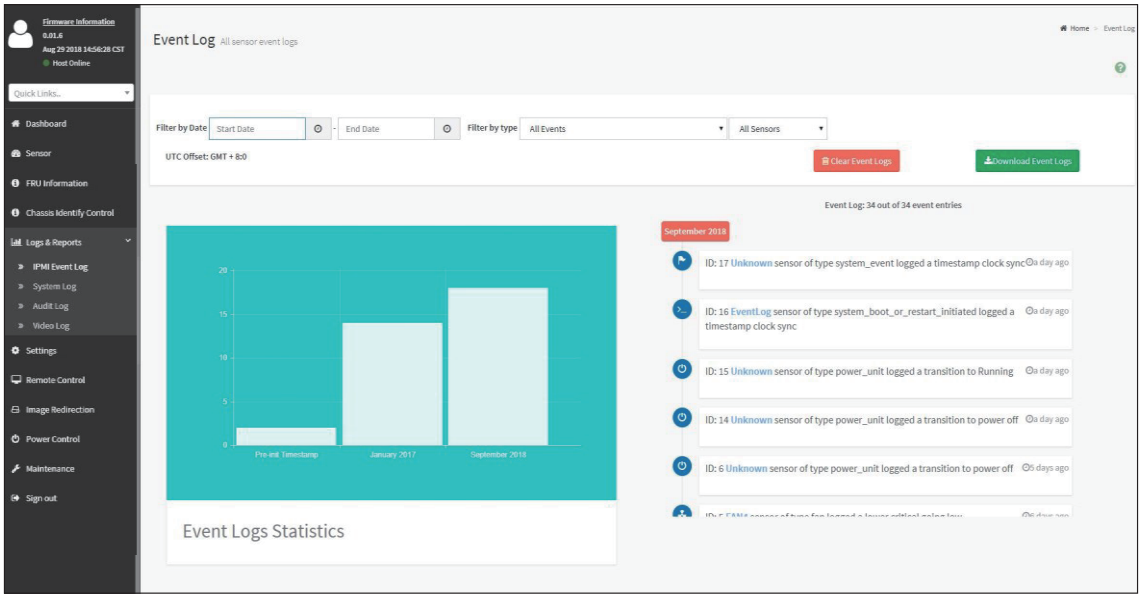
The FRU Information page displays Basic Information, Chassis Information, Board Information, and Product Information of the FRU device. Click **FRU Information** on the menu bar to view the details of the selected device.



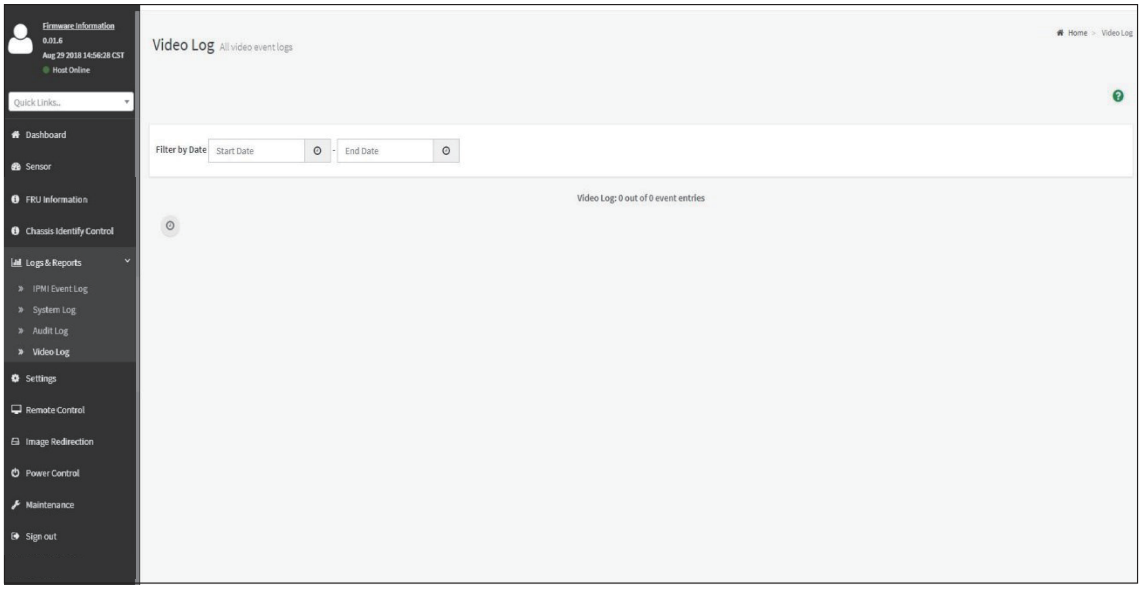
5.2.6 Logs and Report

The System Inventory page displays IPMI Event Log and Video Log. Click **Logs and Reports** from the menu bar and select **Event Log** or **Video Log** to view the contents.

Event Log Page

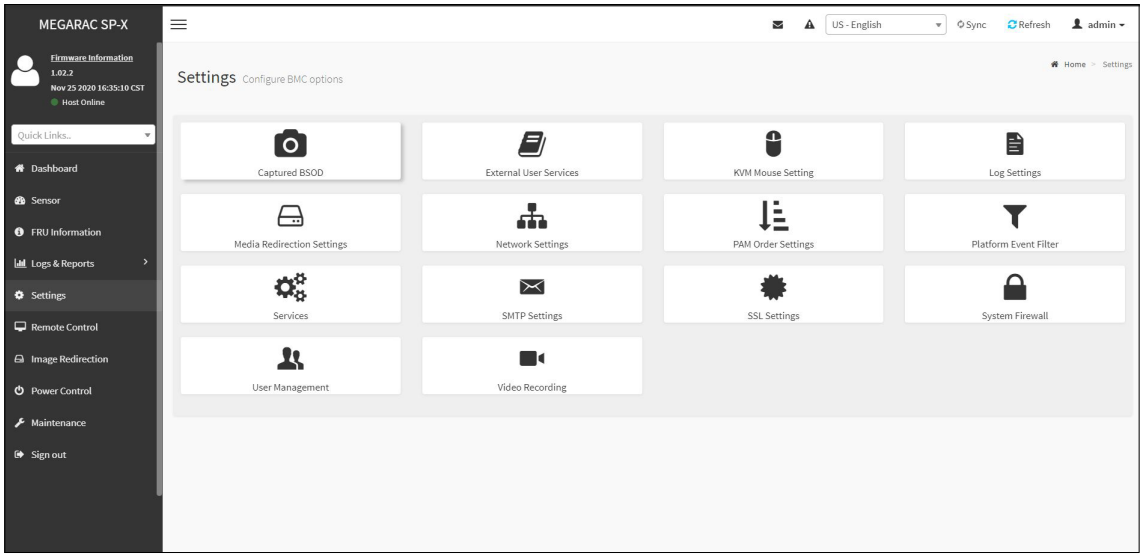


Video Log Page



5.2.7 Settings

The Settings page displays the configuration settings for Captured BSOD, External User Services, KVM Mouse Setting, Log Settings, Media Redirection Settings, Network Settings, PAM Order Settings, Platform Event Filter, Services, SMTP Settings, SSL Settings, System Firewall, User Management, and Video Recording.

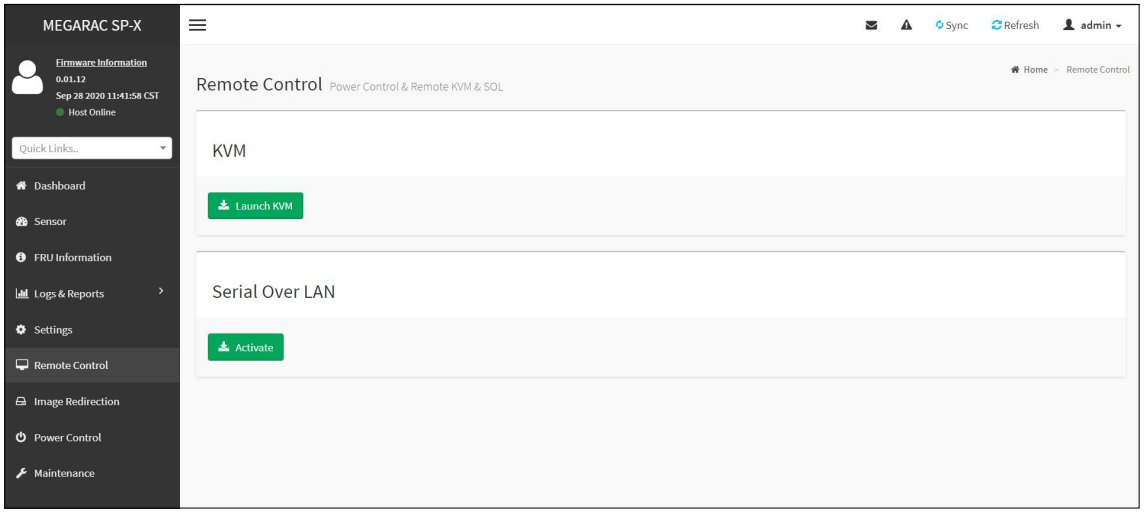


Settings Menu and Option Key:

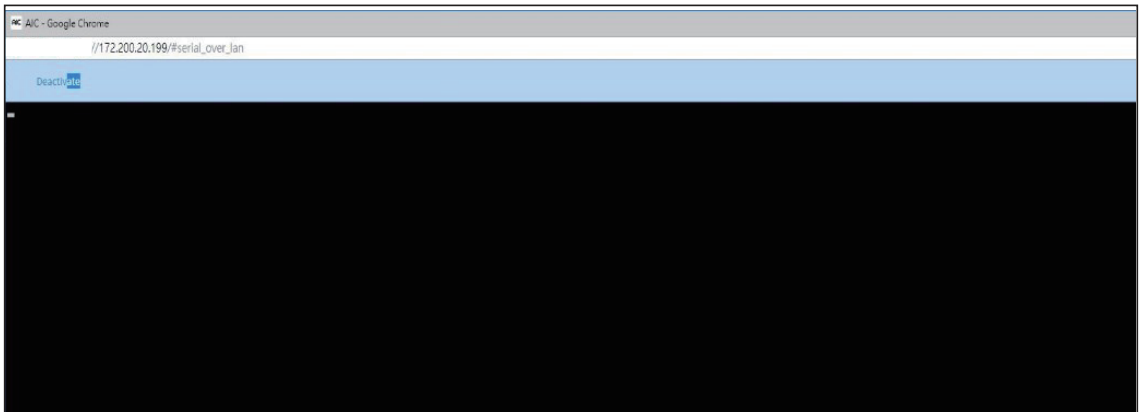
<table>
<tr><th>Settings</th><th colspan="6">Description</th></tr>
<tr><td colspan="7">Captured BSOD</td></tr>
<tr><td rowspan="2">External User Services</td><td colspan="2">LDAP/E-directory Settings</td><td colspan="2">Active directory Settings</td><td colspan="2">Radius Settings</td></tr>
<tr><td>General Settings</td><td>Role Groups</td><td>General Settings</td><td>Role Groups</td><td>General Radius Settings</td><td>Advanced Radius Settings</td></tr>
<tr><td>KVM Mouse Setting</td><td colspan="6">Mouse Mode Configuration
• Relative Positioning (Linux)
• Absolute Positioning (Windows)
• Other Mode (SLES-11 OS Installation)</td></tr>
<tr><td>Log Settings</td><td colspan="3">SEL Log Settings Policy</td><td colspan="3">Advanced Log Settings</td></tr>
<tr><td>Media Redirection Settings</td><td colspan="2">General Settings</td><td colspan="2">VMedia Instance Settings</td><td colspan="2">Active Redirections</td><td>Remote Session</td></tr>
<tr><td>Network Settings</td><td>Network IP Settings</td><td>Network Bond Configuration</td><td colspan="2">Network Link Configuration</td><td>DNS Configuration</td><td>Sideband Interface (NC-SI)</td></tr>
<tr><td>PAM Order Settings</td><td colspan="6">PAM Authentication Order</td></tr>
<tr><td>Platform Event Filter</td><td colspan="2">Event Filters</td><td colspan="2">Alert Policies</td><td colspan="2">LAN Destinations</td></tr>
<tr><td colspan="7">Services</td></tr>
<tr><td>SMTP Settings</td><td colspan="6">SMTP Settings</td></tr>
<tr><td>SSL Settings</td><td colspan="2">View SSL certificate</td><td colspan="2">Generate SSL certificate</td><td colspan="2">Upload SSL certificate</td></tr>
<tr><td rowspan="2">System Firewall</td><td colspan="2">Generate Firewall Settings</td><td colspan="2">IP Address Firewall Rules</td><td colspan="2">Port Firewall Rules</td></tr>
<tr><td>Existing Firewall Settings</td><td>Add Firewall Settings</td><td>Existing IP Rules</td><td>Add New IP rule</td><td>Existing Port Rules</td><td>Add New Port Rule</td></tr>
<tr><td colspan="7">User Management</td></tr>
<tr><td>Video Recording</td><td colspan="2">Auto Video Settings</td><td colspan="2">Video Trigger Settings</td><td colspan="2">Video Remote Settings</td><td>Pre-Event Video Recordings</td></tr>
</table>

5.2.8 Remote Control

The Remote Control page displays the remote KVM and SOL.



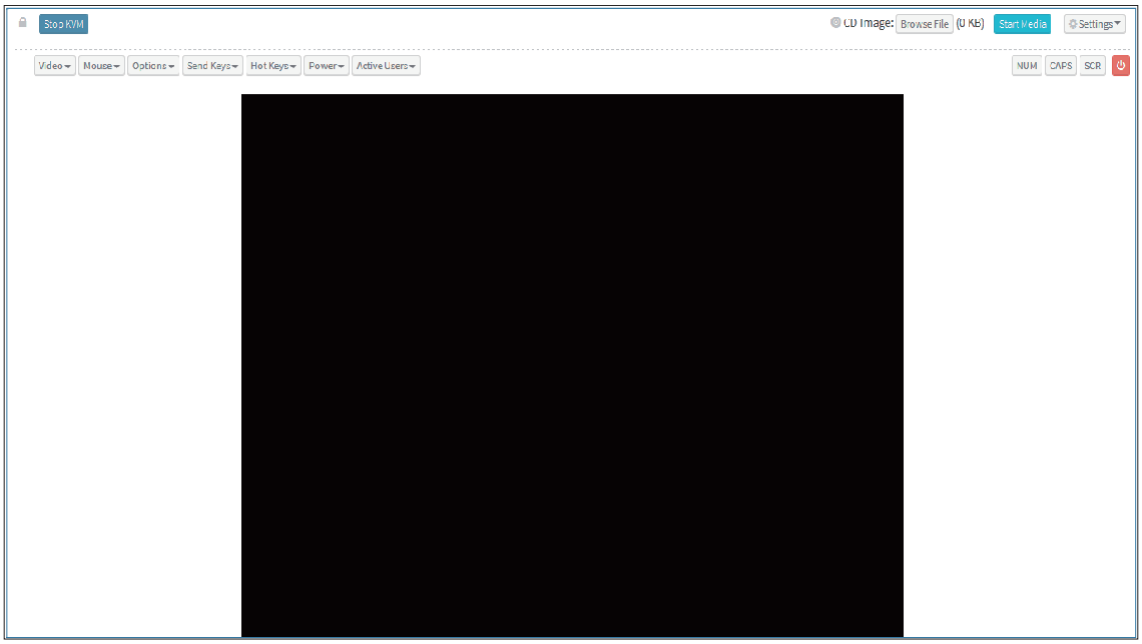
Click **Serial Over Lan** to start the SOL redirection.



Click **Launch KVM** to open the Remote KVM page.

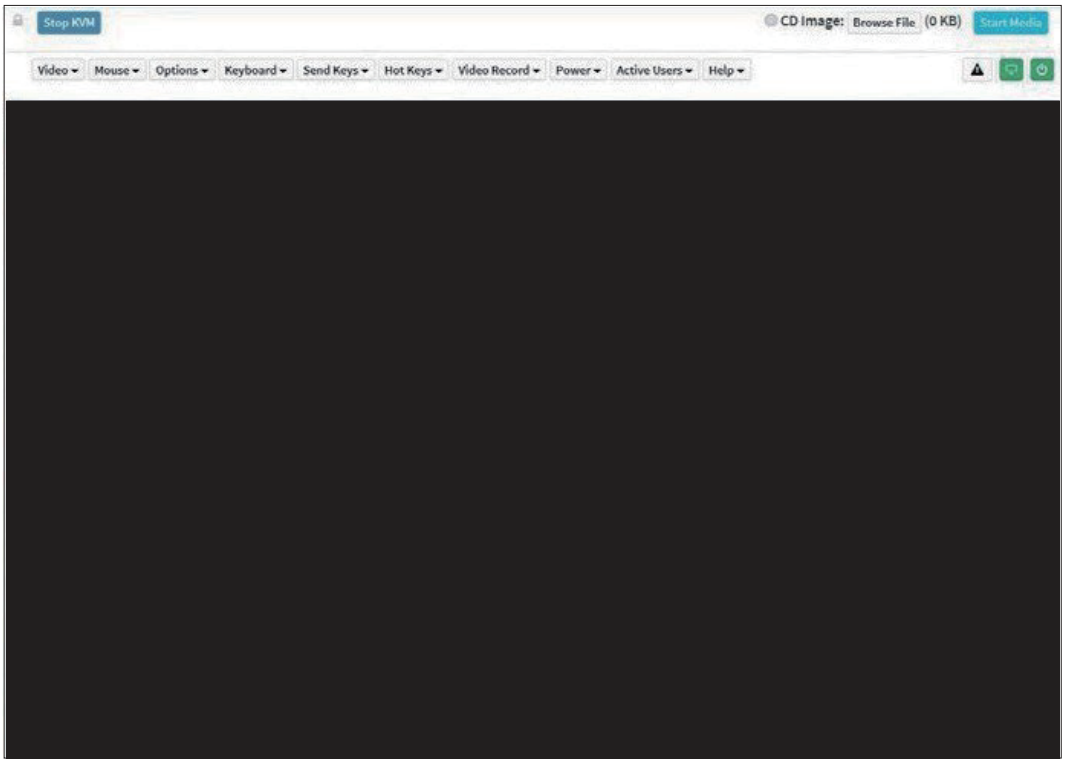
Procedure to Start KVM

Step 1 Click **Start KVM** to start the H5Viewer video redirection.



Step 2 Click **Browse** to select CD Image.

Step 3 Click **Start Media** to redirect the selected CD image file to the Host.



Step 4 To stop the recording, click Stop Record.

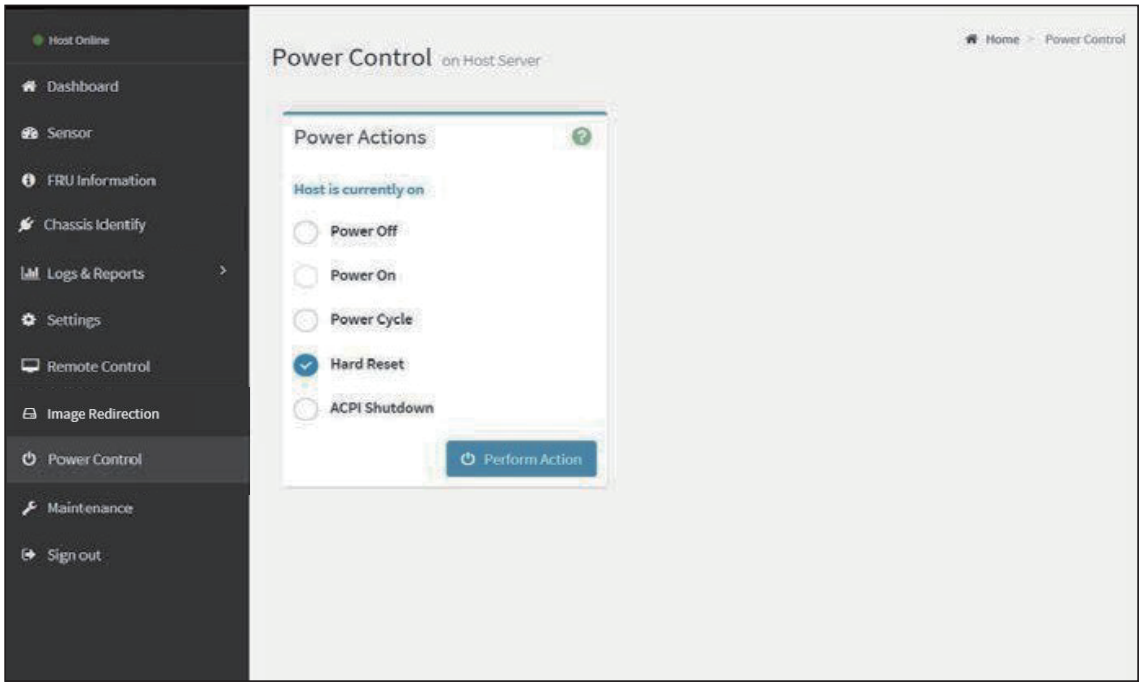
Remote KVM Menu and Option Key:

Remote KVM	Description		
Start KVM	Starts the H5Viewer video redirection.		
Stop KVM	Stops the H5Viewer video redirection.		
Video Record	Pause Video	This option is used for pausing Console Redirection.	
	Resume Video	This option is used to resume the Console Redirection when the session is paused.	
	Refresh Video	This option can be used to update the display shown in the Console Redirection window.	
	Host Display	Display on	If you disable this option, the display will be shown on the screen in Console Redirection.
		Display off	If you enable this option, the server display will be blank but you can view the screen in Console Redirection. If you disable this option, the display will be back in the server screen.
Mouse	Capture Screen	This option helps to take the screenshot of the host screen and save it in the client's system.	
	Show Client Cursor	This menu item can be used to show or hide the local mouse cursor on the remote client system.	
	Mouse Mode	This option handles mouse emulation from local window to remote screen using either of the two methods. Only 'Administrator' has the right to configure this option. • Absolute mouse mode: The absolute position of the local mouse is sent to the server if this option is selected. • Relative mouse mode: The Relative mode sends the calculated relative mouse potion displacement to the server if this option is selected. • Other mouse mode: This mouse mode sets the client cursor in the middle of the client system and will send the deviation to the host. This mouse mode is specific for SUSE Linux installation.	
	NOTE Client cursor will be hidden always. If you want to enable, use Alt + C to access the menu.		
Options	Block Privilege Request	To enable or disable the access privilege of the user.	
	Keyboard/ Mouse Encryption	This option allows you to encrypt keyboard inputs and mouse movements sent between the connections	
Keyboard	Keyboard Layout	List of Host Physical Keyboard languages supported in H5Viewer. 1. English US 2. German 3. Japanese	
Video Record	Record Video	This option is to start recording the screen.	
	Stop Recording	This option is used to stop the recording.	
	Record Settings	This option is used to set Video Recording Duration.	

Send Keys	Hold Down	Right <Ctrl>	This menu item can be used to act as the right-side <CTRL> key during Console Redirection.
		Right <Alt>	This menu item can be used to act as the right-side <ALT> key during Console Redirection.
		Right <Window>	This menu item can be used to act as the right-side <WIN> key during Console Redirection.
		Left <Ctrl>	This menu item can be used to act as the left-side <CTRL> key during Console Redirection.
		Left <Alt>	This menu item can be used to act as the left- side <ALT> key during Console Redirection.
		Left <Window>	This menu item can be used to act as the left- side <WIN> key during Console Redirection. You can also decide how the key should be pressed: Hold Down or Press and Release.
	Press and Release	<Ctrl> + <Alt> + <Del>	This menu item can be used to act as if you depressed the <CTRL>, <ALT>, and <DEL> keys down simultaneously on the server that you are redirecting.
		Left <Windows>	This menu item can be used to act as the left- side <WIN> key during Console Redirection. You can also decide how they key should be pressed: Hold Down or Press and Release.
		Right <Windows>	This menu item can be used to act as the right-side <WIN> key during Console Redirection.
		<Context Menu>	This menu item can be used to act as the context menu key, during Console Redirection.
		<Print Screen>	This menu item can be used to act as the print screen key, during Console Redirection.
Hot Keys	Add Hot Keys	This menu is used to enable macros. Click Add to macros.	
Power	Power Reset	To reboot the system without powering off (warm boot).	
	Immediate Shutdown	Power Off the server immediately.	
	Orderly Shutdown	Soft power off.	
	Power On	To power on the server.	
	Power Cycle	To first power off and then reboot the system (cold boot).	
Active Users	Read only. Displays active user and their system IP address.		
Help	Read only. Displays information about H5viewer.		

5.2.9 Power Control

The Power Control page allows you to view and control the power of your server. To open Power Control, click **Power Control** from the menu bar.



The various options of Power Control are given below.

Power Off: To immediately power off the server.

Power On: To power on the server.

Power Cycle: This option will first power off and then reboot the system (cold boot).

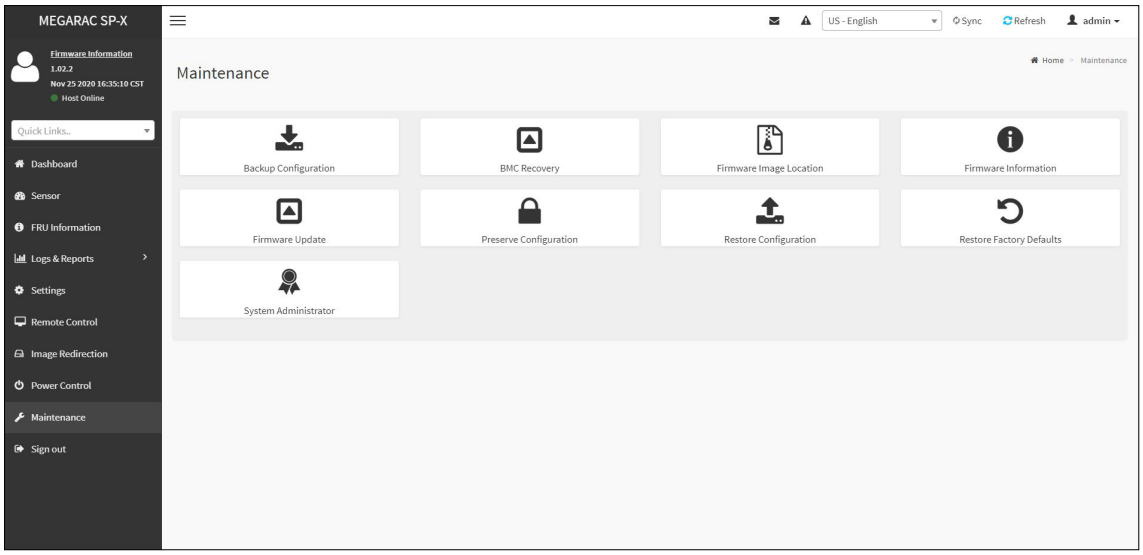
Hard Reset: This option will reboot the system without powering off (warm boot).

ACPI Shutdown: This option to initiate operating system shutdown prior to the shutdown.

Perform Action: Click this option to perform the selected operation.

5.2.10 Maintenance

This Maintenance page displays the configuration settings for Backup Configuration, Firmware Image Location, Firmware Information, Firmware Update, Preserve Configuration, Restore Configuration, and Restore Factory Defaults.



Maintenance	Description
Backup Configuration	1. Click Check All to backup the selected configuration items. The Backup Configuration page will appear Click Download Config to save the backup file to the client system. 2. Click OK to perform the backup action. The Backup file will be saved in the client system. 3. Click Cancel to cancel the backup process.
Firmware Image Location	1. Click the configuration items on the list. 2. Click **Save** to save any changes made.
Firmware Information	Read only.
BMC Recovery	1. Choose Enable/Disable to start auto-recovery immediately at next reboot. 2. Enter the number of retries to reset the BMC and this count ranges from 1 to 5. 3. Enter the number of retries to recover firmware image during the recovery process and this count ranges from 1 to 5. 4. Address of the server where the firmware image is stored. • IP Address made of 4 numbers separated by dots as in xxx.xxx.xxx.xxx. • Each number ranges from 0 to 255. • First number must not be 0. 5. Enter the Image Name to edit the default recovery image name is mentioned as rom.ima. • Image name should contain only 10 characters.
Firmware Update	This wizard takes you through the process of firmware upgradation. A reset of the box will automatically follow if the upgrade is completed or cancelled. An option to Preserve All Configuration is available. Enable it, if you wish to preserver configured settings through the upgrade. Click **Start Firmware Update** to start the firmware update process.
Preserve Configuration	This page allows the user to configure the preserve configuration items, which will be used by the Restore factory defaults to preserve the existing configuration without overwriting with defaults/Firmware Upgrade configuration. Click **Save** to save any changes made.
Restore Configuration	1. Click **Upload** to restore the backup files. 2. Click **OK** to upload the new configuration file and restore.
Restore Factory Defaults	1. Click the configuration items on the list to preserve the settings during restore factory default configuration. 2. Click **Restore Factory Defaults** to restore the factory defaults of the device firmware.
System Administrator	Modified administrator account information

5.2.10.1 Firmware Update

This wizard takes you through the process of firmware upgradation. A reset of the box will automatically follow if the upgrade is completed or cancelled. An option to Preserve All Configuration is available. Enable it, if you wish to preserve configured settings through the upgrade.

Warning: Please note that after entering update mode widgets, other web pages and services will not work. All open widgets will be closed automatically. If upgrade process is cancelled in the middle of the wizard, the device will be reset.

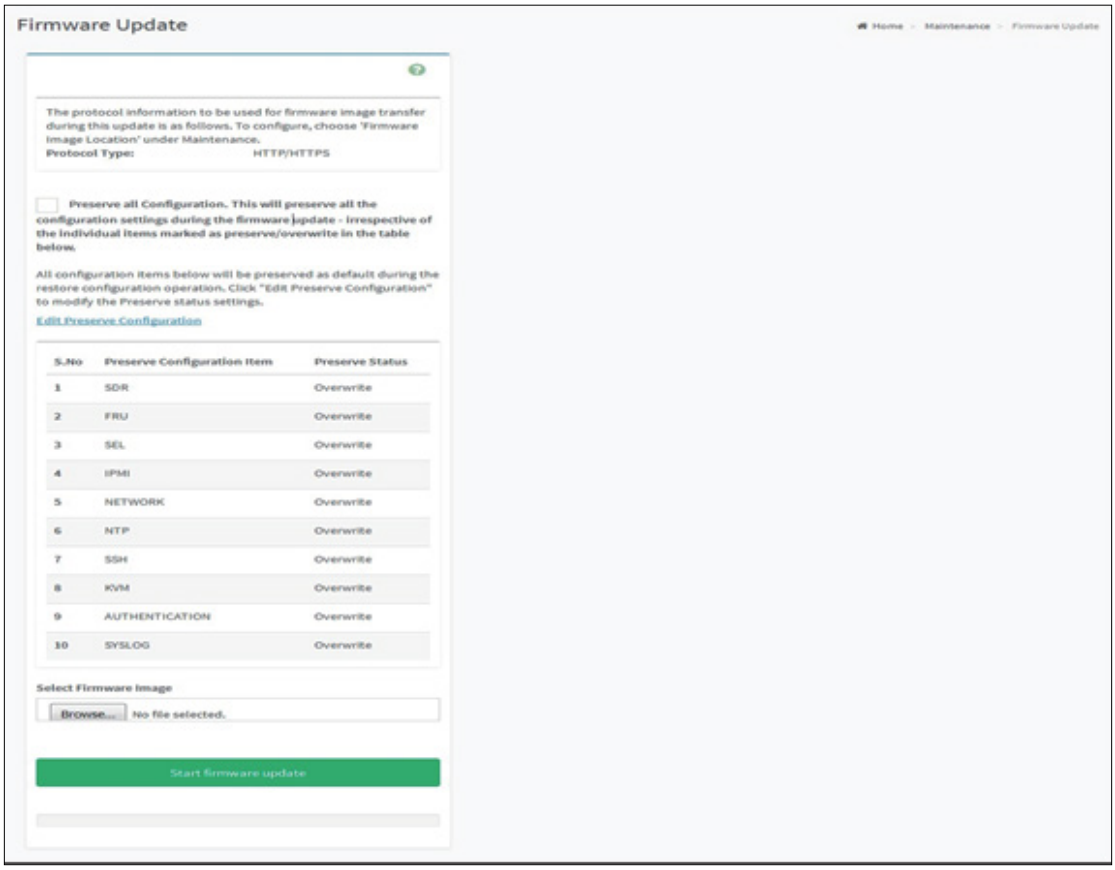
NOTE

The firmware upgrade process is a crucial operation. Make sure that the chances of a power or connectivity loss are minimal when performing this operation.

Once you enter into Update Mode and choose to cancel the firmware flash operation, the MegaRAC® card must be reset. This means that you must close the Internet browser and log back onto the MegaRAC® card before you can perform any other types of operations.

Once Firmware upgrade using web is started, the regular IPMI command will not be allowed for safety concern if Enable IPMI Command handling during flashing support is disabled in project configuration.

To configure, choose Firmware Image Location under Maintenance. To open Firmware Update page, click Maintenance → Firmware Update from the menu bar.



Firmware Update page

The various fields of Firmware Update are as follows.

- Preserve all Configuration: To preserve all configuration.
- Edit Preserve Configuration: To modify the Preserve status settings.
- Select Firmware Image: To Select the Firmware image to be uploaded.
- Start Firmware Update: To Start the Firmware Update.

This wizard takes you through the process of AMI based firmware upgradation. The protocol information to be used for firmware image transfer during this update is as follows.

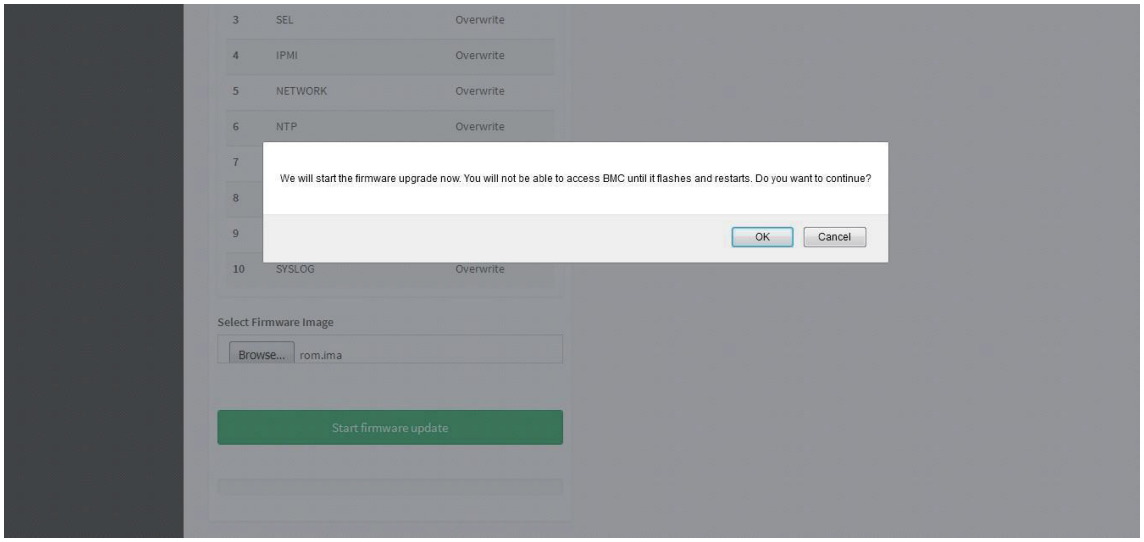
> **NOTE**
> All configuration items will be preserved/overwrite as default during the restore configuration operation.

Procedure

1. Click Preserve all Configuration to preserve all configuration.
2. Click Browse to select firmware image. The Firmware update undergoes the following steps:
   a. Closing all active client requests
   b. Preparing Device for Firmware Upgrade
   c. Uploading Firmware Image

> **NOTE**
> A file upload pop-up will be displayed for http/https but in the case of tftp files, the file is automatically uploaded displaying the status of upload.

   d. Browse and select the Firmware image to flash and click Upload.
   e. Click Start firmware update start the Firmware Update. A warning message will be prompted you to proceed further.
   f. Click OK to start the Firmware Update. The sample screenshot is shown below.



Firmware Update page - Image Upload

g. Verifying Firmware Image

In Section Based Firmware Update, you can configure the firmware image for section based flashing. Check the required sections and click Proceed to update the firmware.

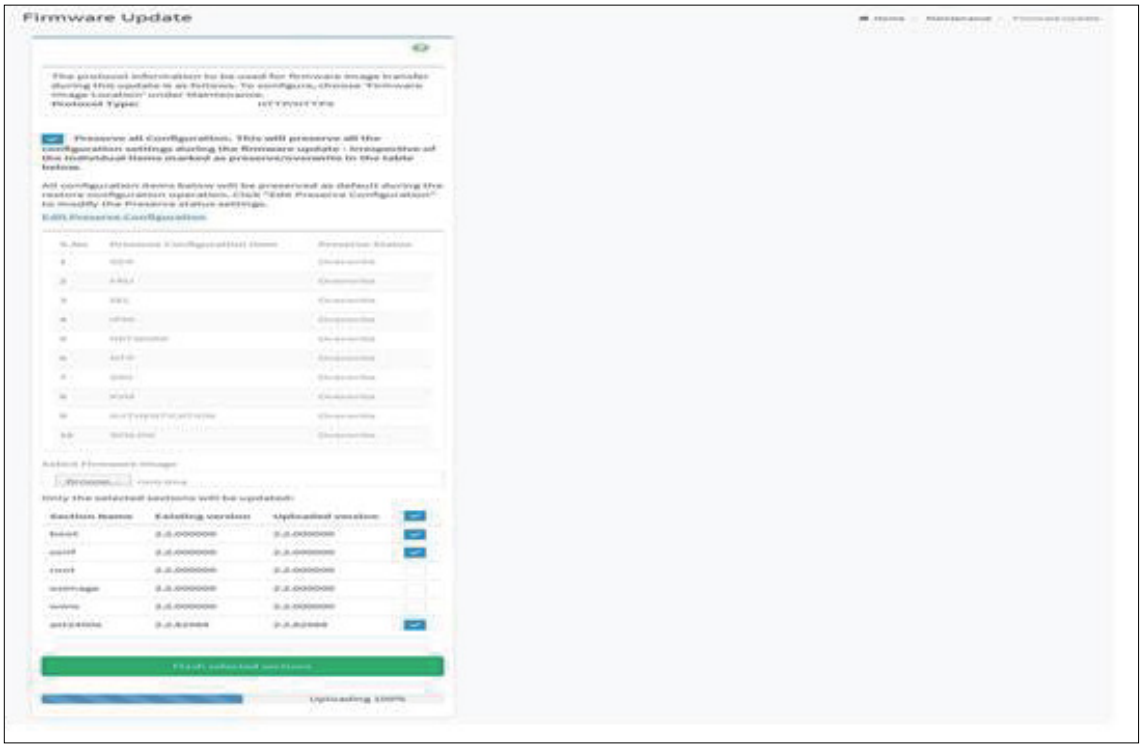
If flashing is required for all images, select the option Full Flash .

If you select Version Compare Flash option from web, the current and uploaded module versions, FMHlocation, size will be compared.

If the modules differ in size and location, proceed with force firmware upgrade. If all the module versions are same, restart BMC by saying all the module versions are similar.

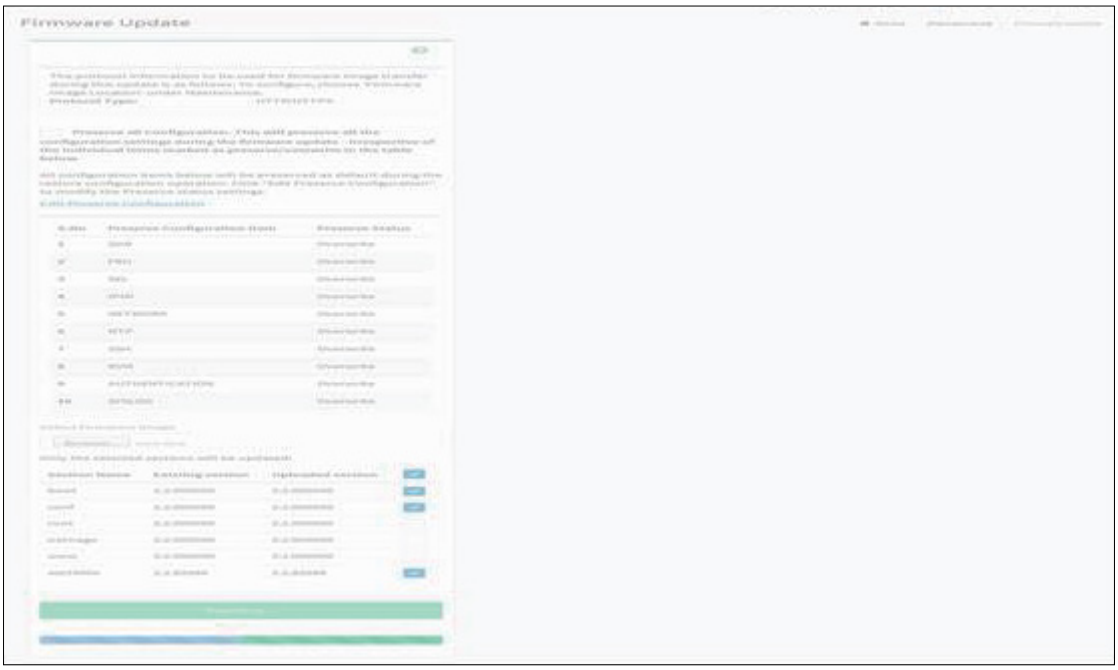
If only few module versions are differ, those module will be flashed.

NOTE
Only selected sections of the firmware will be updated. Other sections are skipped. Before starting flash operation, you are advised to verify the compatibility between image sections.



Section Based Firmware Flashing

h. Flashing Firmware Image
i. Resetting the image. The sample screenshot of Firmaware update is as shown below.



Firmware Update page

NOTE
The Firmware Update page will be disabled and you will not be able to perform any other tasks until firmware upgrade is completed and the device is rebooted. You can now follow the instructions presented in the subsequent pages to successfully update the card's firmware. The device will reset if update is canceled. The device will also reset upon successful completion of firmware update.

5.2.10.2 BIOS Firmware Update

Remote update BIOS firmware via BMC guide

- Yafuflash

1. a. Boot to Linux.

b. Enter BMC firmware directory [xxxxzzzz] ;

xxxx:project name ;

zzzz:firmware version ;

c. Copy BIOS firmware file (*.bin) to linux folder.

Example:

Linux x64

cp bios.bin SB203LX010005/Linux/

Linux x86

cp bios.bin SB203LX010005/Linux32/

d. Shutdown the host or remote send power off system command.

ipmitool -I lanplus -H <BMC_IP> -U [username] -P [password] power off

e. Execute update BIOS command

Linux x64

cd SB203LX010005/Linux/

./Yafuflash64 -nw -u [username] -p [password] -ip <BMC_IP> -d 2 bios.bin

Linux x86

cd SB203LX010005/Linux32/

./Yafuflash32 -nw -u [username] -p [password] -ip <BMC_IP> -d 2 bios.bin

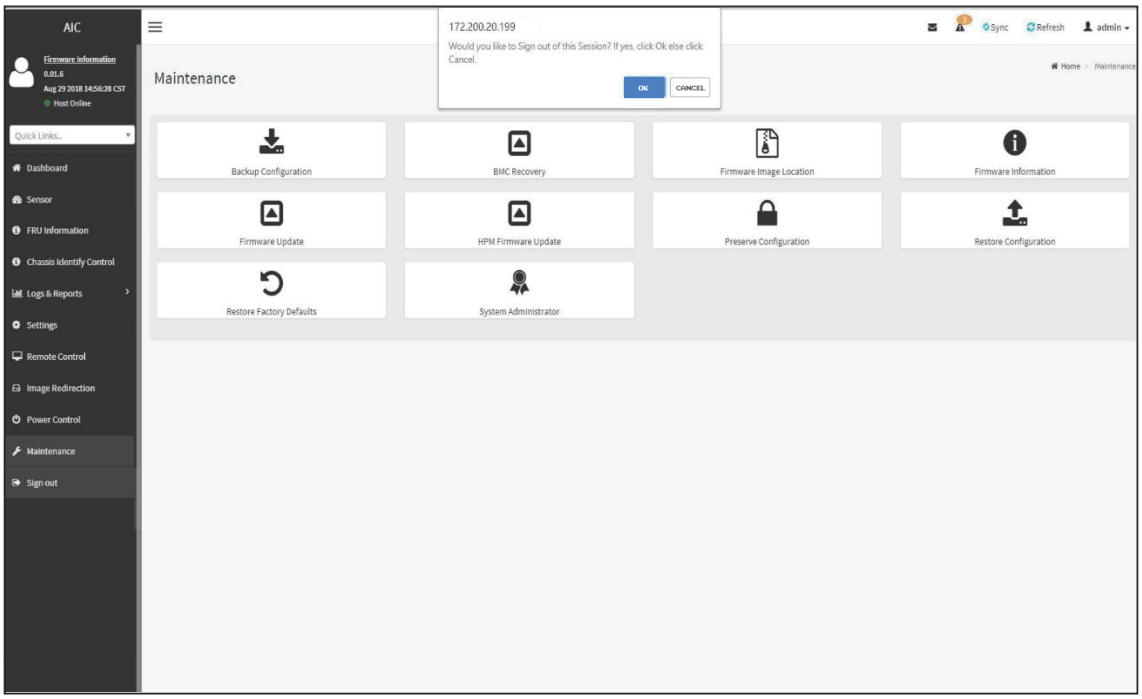
NOTE
This is just an example, "SB203LX010005" is BMC firmware file name.
Please instead "SB203LX010005" to your BMC firmware directory name.
“bios.bin” is BIOS firmware file name, please instead "bios" to your BIOS firmware file name.
[username] and [password] are the same as IPMI.

NOTE
Please change your account to root, or you will get an exception fail.

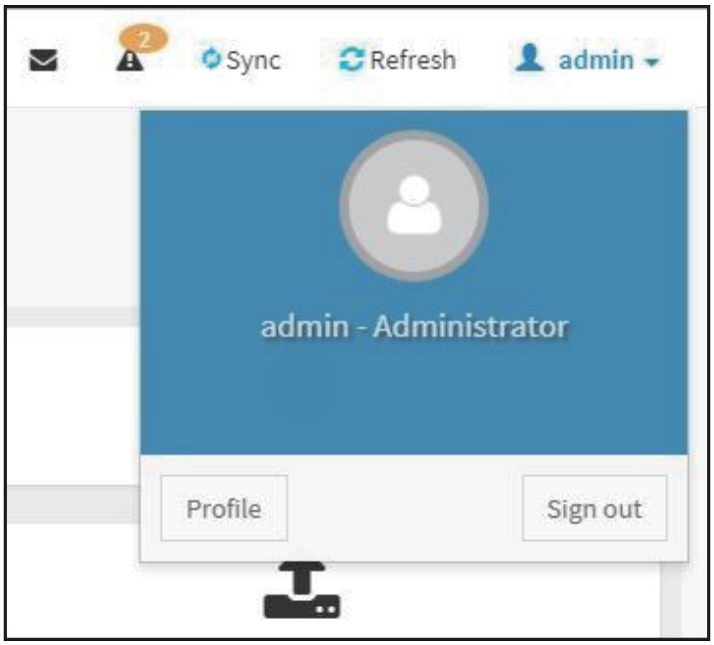
5.2.11 Sign out

To log out of the BMC:

Method 1: Click Sign out from the menu bar. The Logout dialog box will pop out.



Method 2: Click the root quick button on the top right corner of the screen.



NOTE
For further details about the BMC, please refer to BMC section in the Auriga manual for reference.
AIC® website link: https://www.aicipc.com/en/productdetail/50929.

Chapter 6. Technical Support

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