Auriga

Server Motherboard
User's Manual

UM_Auriga_v2_010322

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Document Release History

Release Date	Version	Update Content
October, 2018	1	User's Manual release to public.
March, 2019	1.1	1. BMC update 2. H/W spec update
April, 2019	1.2	H/W update
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Preface

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Changes

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Warning

1. A shielded-type power cord is required in order to meet FCC emission limits and also to prevent interference to the nearby radio and television reception. It is essential that only the supplied power cord be used.
2. Use only shielded cables to connect I/O devices to this equipment.
3. You are cautioned that changes or modifications not expressly approved by the party responsible for compliance could void your authority to operate the equipment.

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Instruction Symbols

Special attention should be given to the instruction symbols below.

NOTE	This symbol indicates that there is an explanatory or supplementary instruction.
CAUTION	This symbol denotes possible hardware impairment. Upmost precaution must be taken to prevent serious harware damage.
WARNING	This symbol serves as a warning alert for potential body injury. The user may suffer possible injury from disregard or lack of attention.

Safety Instructions

When installing, operating, or performing maintenance on this equipment, the following safety precautions should always be taken into account in order to reduce the risk of fire, electric shock, and personal injury.

Carefully read the safety instructions below before using this product.

- Observe all of the warning and instruction signs distinctively marked on the product.
- Before performing system installations, please consult the User's Manual provided with this product.
- Do not place this product on an uneven or weak surface (unstable cart, stand, table, ect.) that might induce the product to fall and sustain serious damage.
- Install only the equipment or device identified in the User's Manual. Deploying other equipment or device with this motherboard could invoke improper connection of circuitry that leads to fire or personal injury.
- This product should only be operated with the type of power source indicated on the marked label. If you are questionable about which type of power supply is used in your area, consult your dealer or local Power Company.
- Disconnect the power supply module before removing power from the system.
- Unplug this product from the wall outlet before cleaning. Use a damp cloth for cleaning. Do not use liquid cleaners or aerosol cleaners.
- Do not use this product near a water source, including faucet and lavatory.
- Never spill liquids of any kind on this product.
- Never shove objects of any kind into this product's open slots, as they may touch dangerous voltage points or short out parts and could result in fire or electric shock.
- Do not block or cover slots and openings in this unit, as they were made for ventilation and prevent this unit from overheating. Do not place this product in a built-in installation unless proper ventilation is available.
- Do not disassemble this product. This product should only be taken apart by trained personnel. Opening or removing covers and circuit boards may expose you to electric shock or other risks. Incorrect reassembly can also cause electric shock when the unit is subsequently used.
- Risk of explosion is possible if battery is replaced with an incompatible type. Dispose of used batteries accordingly.
- This product is equipped with a three-wire grounding type plug, a plug with a third (grounding) pin. As a safety feature, this plug is intended to fit only into a grounding type power outlet. If you are unable to insert the plug into the outlet, contact your electrician to replace the outlet. Do not remove the grounding type plug or use a 3-Prong To 2-Prong Adapter to circumvent the safety feature; doing so may result in electric shock and/or damage to this product.

About This Manual

Thank you for selecting and purchasing the Auriga Serverboard.

This user's manual is provided for professional technicians to perform easy hardware setup, basic system configurations, and quick software startup. This document pellucidly presents a brief overview of the product design, device installation, and firmware settings for the Auriga motherboard. For the latest version of this user's manual, please refer to the AIC® website: https://www.aicipc.com/en/productdetail/50929.

Chapter 1 Product Features

This chapter delivers the overall layout of the product, including the fundamental components on the motherboard, design specifications, and noteworthy features. Auriga is an ideal server grade motherboard that is specifically designed to accommodate diverse enterprises for managing heavy workloads, databases, nearline applications, and cloud deployments. This product supports the single AMD EPYC™ 7000-series processor and Socket SP3 socket type with a memory support of 8 channel DDR4 RDIMM/LRDIMM/NVDIMM-N with EEC up to 2667 MHz.

Chapter 2 Hardware Setup

This chapter displays an easy installation guide for assembling the CPU (Central Processing Unit) and memory module. Utmost caution for proceeding to set up the hardware is highly advised. The components on the motherboard are highly fragile and vulnerable to exterior influence. Do not attempt to endanger the device by placing the device in a potentially unstable or hazardous surroundings, including positioning the device on an uneven grounds or humid environments.

Chapter 3 Motherboard Settings

This chapter elaborates the overall layout of the server motherboard, including multifarious connectors, jumpers, and LED descriptions. These descriptions assist users to configure different settings and functions of the motherboard, as well as to confirm the placement of each connector and jumper.

Chapter 4 BIOS Configuration Settings

This chapter introduces the key features of BIOS, including the descriptions and option keys for diverse functions. These details provide users to effortlessly navigate and configure the input/output devices.

Chapter 5 BMC Configuration Settings

This chapter illustrates the diverse functions of IPMI BMC, including the details on logging into the web page and assorted definitions. These descriptions are helpful in configuring various functions through Web GUI without entering the BIOS setup. For more information of BMC configurations, please refer to IPMI BMC (Aspeed AST2500) User's Manual for a more detailed description.

Chapter 6 Technical Support

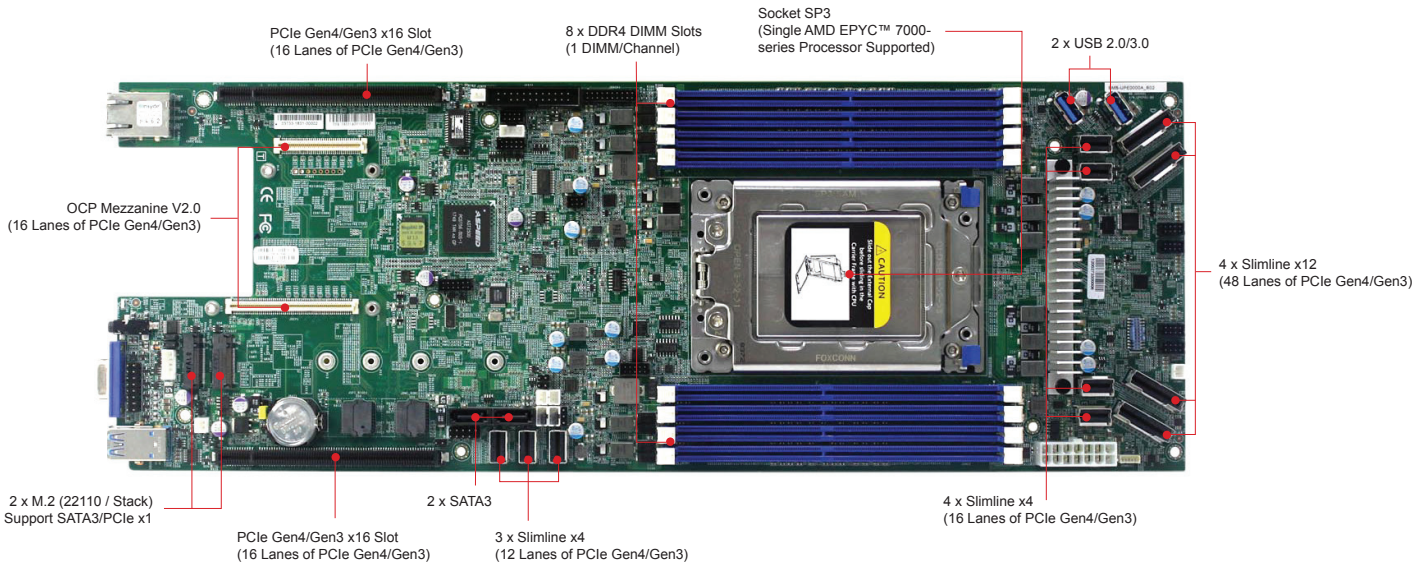
For more information or suggestion, please contact the nearest AIC® corporation representative in your district or visit the AIC® website: https://www.aicipc.com/en/index. It is our greatest honor to provide the best service for our customers.

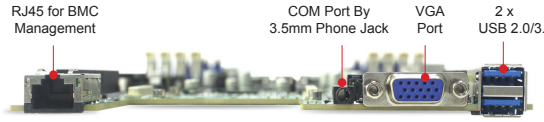
Chapter 1. Product Features

This section describes the hardware specifications and features of the Auriga motherboard. The fundamental components of the Auriga severboard are provided below.

1.1 Component

Auriga Serverboard





Dimensions

mm : 431.8 x 157.4
inches : 17 x 6.2

Product specifications and features are subject to change without prior notice.

1.2 Specifications

System	Processor Support	Single AMD EPYC™ 7003/7002/7001 processor
	CPU TDP	280W (support by EPYC™ 7003 CPU)
	Socket Type	Socket SP3
	System Memory	• DDR4 3200/2933/2666MHz RDIMM/LRDIMM • Total 8 memory slots ; 8 channels • Supports up to 2TB (support by EPYC™ 7003/7002)
	Expansion Slots	• 4 x Slimline x12 + 7 x Slimline x4 • 2 x PCI Express Gen4/Gen3 x16 slots (Gen4 supported by EPYC™ 7003/7002 CPU) • 1 x OCP Mezzanine V2.0 supports PCI Express Gen4/Gen3 x16 (Gen4 supported by EPYC™ 7003/7002 CPU) Total support 124 lanes of PCI Express Gen4/Gen3 (Gen4 supported by EPYC™ 7003/7002 CPU) • 2 x NGFF(M.2) M-Key(2242/2260/2280/22110) support SATA/PCIe x1
System BIOS	BIOS Type	EPYC 7003/7002/7001 – UEFI BIOS
	BIOS Features	• ACPI • PXE • IPMI KCS interface • SMBIOS • SRIOV • Serial console redirection • iSCSI • TPM • PCIe Hotplug
On-board Devices	SATA/NVMe	• 2 x SATA 6.0 Gb/s • 2 x SATA 6.0 Gb/s by M.2 (M-key) support up to 22110 (optional - above 4 SATA ports can be replaced with 2 x PCIe x1 M.2)

On-board Devices	BMC	Aspeed AST2500 Advanced PCIe Graphics & Remote Management Processor • Baseboard Management Controller • Intelligent Platform Interface 2.0 (IPMI 2.0) • iKVM, Media Redirection, IPMI over LAN, Serial over LAN • HTML5 • Redfish • SMASH Support
	Graphics	Aspeed AST2500 Advanced PCIe Graphics & Remote Management Processor • PCIe VGA/2D Controller • 1920x1200@60Hz 32bpp
Input/Output	SATA/NVMe	• 2 x SATA 6.0 Gb/s • 2 x SATA 6.0 Gb/s by M.2 (M-key) supports up to 22110 (optional - above 4 SATA ports can be replaced with 2 x PCIe x1 M.2)
	LAN	• 1 x GbE RJ45 dedicated to BMC management
	USB	• 2 x USB2.0/3.0 Type A connectors on rear I/O • 2 x USB2.0/3.0 by onboard vertical Type A connectors
	VGA	• 1 x external VGA port • 1 x internal VGA pin-header (share with external VGA port)
	Serial Port	• 1 x external COM port by 3.5mm phone jack • 1 x internal COM pin-header
	Others	• 1 x TPM 2.0 onboard

NOTE

Please refer to the processor type (AMD EPYC™ 7003/7002/7001) on your serverboard for the corresponding firmware information.

- If the AMD processor generation is EPYC™ 7003, the serverboard executes with AMI UEFI BIOS.
- If the AMD processor generation is EPYC™ 7002/7001, the serverboard executes with Insyde UEFI BIOS.

1.3 Feature

The Auriga server board offers the latest AMD EPYC™ SoC technology which can support the highest core count in an x86-architecture with EPYC™ 7003/7002/7001 processor, more main memory capacity and bandwidth with greater efficiency and greatest I/O density.

Auriga has I/O bandwidth that matches the capability of the CPU cores to move data to and from the network, spinning disks, NVMe storage, and graphics acceleration devices. By offering the parallelism to speed high performance computing environments, machine learning and predictive analysis benefit from the capability to process more data in memory and to accelerate computation with
more direct GPU connectivity.

- Supports AMD EPYC™ 7003/7002/7001 processor based on the AMD “Zen” microarchitecture for highest server performance
- Supports eight DDR4 DIMM slots for maximum memory performance
- Supports one OCP Mezzanine V2.0 up to PCI Express Gen4/Gen3 x16 extension (Gen4 supported by EPYC™ 7003/7002 CPU)
- Supports two PCI Express Gen4/Gen3 x16 slots (Gen4 support by EPYC™ 7003/7002 CPU)
- Supports four slimline x12 + seven slimline x4 connectors, total 76 PCI Express Gen4/Gen3 lanes (Gen4 supported by EPYC™ 7003/7002 CPU)
- Onboard Baseboard Management Controller for system management and IPMI control
- Embedded components for 5+ year long life
- Rackmount Technology Extension (RTX) form factor utilizes full internal chassis volume for optimum I/O configurations

Chapter 2. Hardware Setup

This section describes a simple instruction guide for installing the hardware components on the serverboard system. Turn off and unplug all system and peripheral devices before proceeding.

2.1 Central Processing Unit Setup

The serverboard supports a single AMD EPYC™ 7000-series and socket type SP3.

2.1.1 Processor Installation

To ensure a safe and easy setup, you need to prepare before installation:

☑ a T20 Torx screwdriver

☑ ESD wrist strap/mat and conductive foam pad

CAUTION
The pins of the processor socket are vulerable and easily susceptible to damage if fingers or any foreign objects are pressed against them. Please keep the socket protective cover on when the processor is not installed.

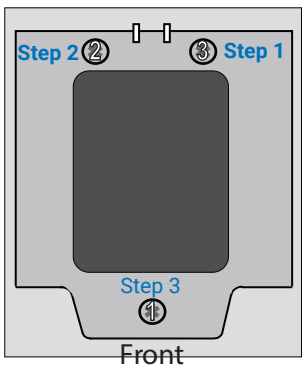
CAUTION
When unpacking a processor, hold the processor only by its edges to avoid touching the contacts.

Procedure:

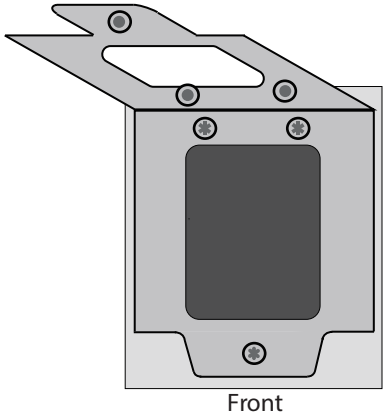
① Remove the screw in the order designated in blue (the screw labeled 3、2、1) as demonstrated in figure 1. After the screws are dislodged, the load plate will automatically be ejected as demonstrated in figure 2.

NOTE
The screws cannot be completely removed from the CPU cover.

Dislodge screw



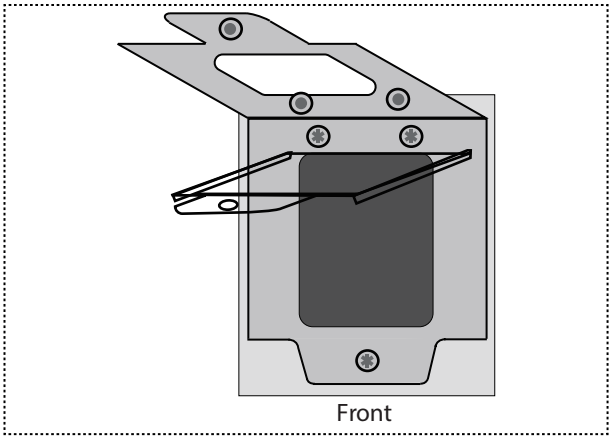
Remove top cover



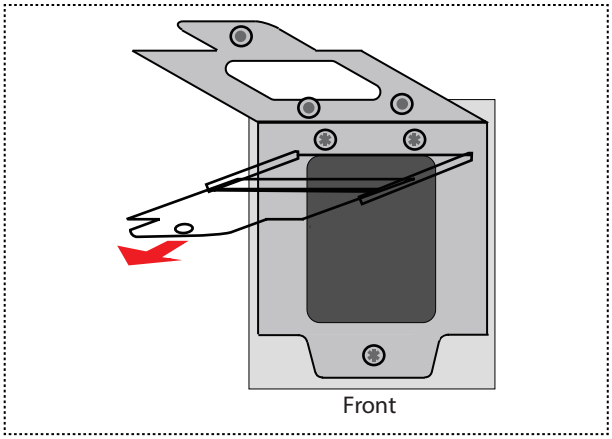
This information is provided for professional technicians only.

② Lift the carrier frame by the blue metal tab and remove the protective cover as demonstrated in figure 3 and figure 4.

Lift carrier frame

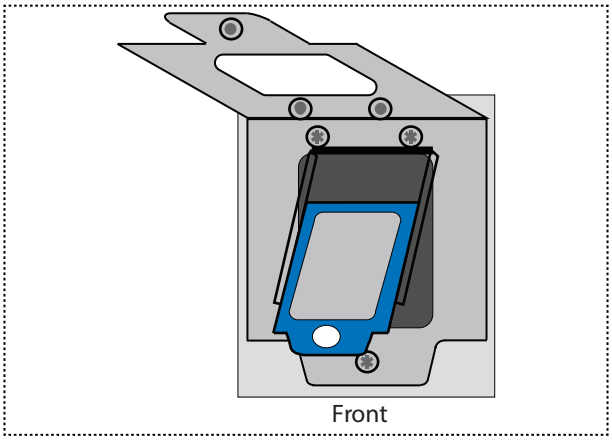


Remove protective cover



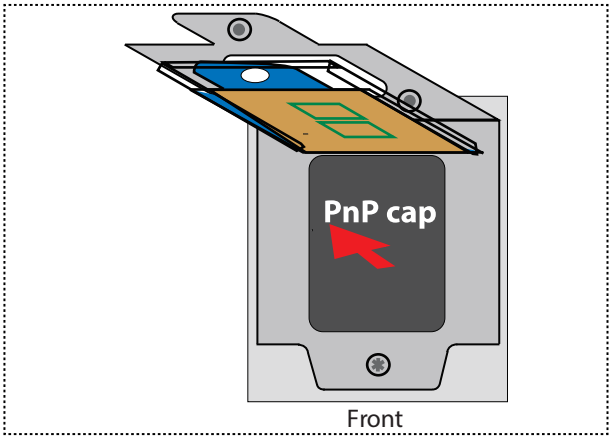
③ Insert the CPU package into the carrier frame as demonstrated in figure 5.

Insert package



④ Remove the Pick and Place(PnP) cap by lifting the it upward as demonstrated in figure 6.

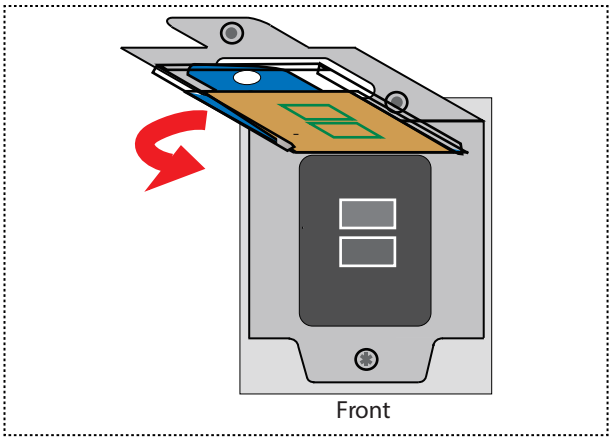
Lift PnP cap



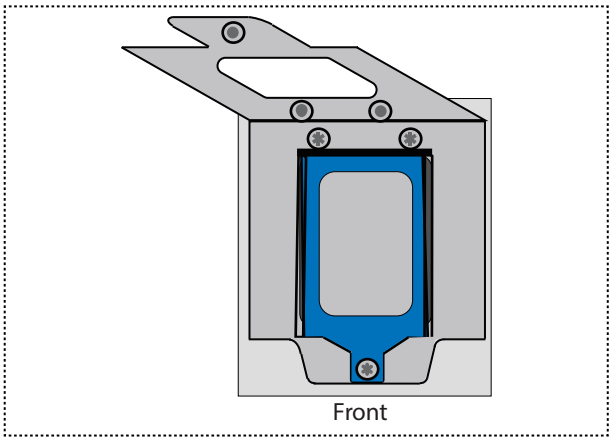
This information is provided for professional technicians only.

⑤ Close the carrier frame with the CPU package as demonstated in figure 7. Check if the frame is properly installed as demonstrated in figure 8.

Close carrier frame

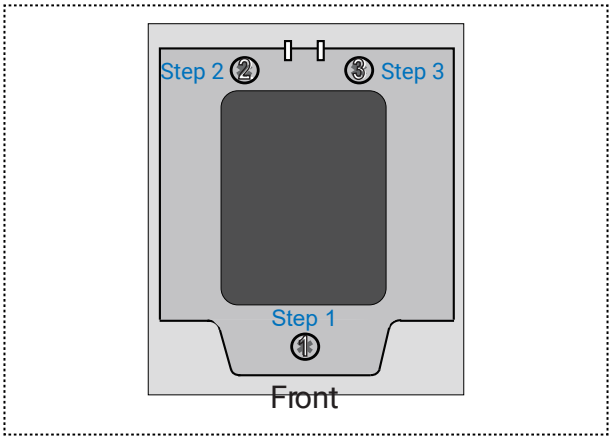


Verify installation



⑥ Close the load plate and fasten the screws in the order 1→2→3 to complete installation as demonstrated in figure 9.

Close load plate



⑦ Apply thermal grease/paste on top of the CPU assembly.

⑧ Secure the heatsink on top of the processor assembly to complete installation.

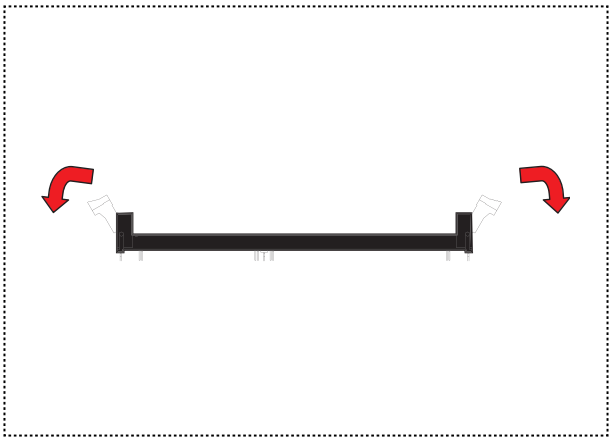
This information is provided for professional technicians only.

2.2 System Memory Setup

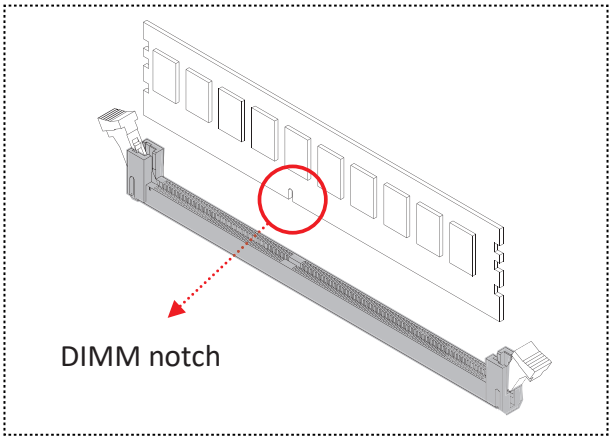
This server board supports 8 DIMM memory slots with 1 DIMM per channel.

2.2.1 DIMM Installation

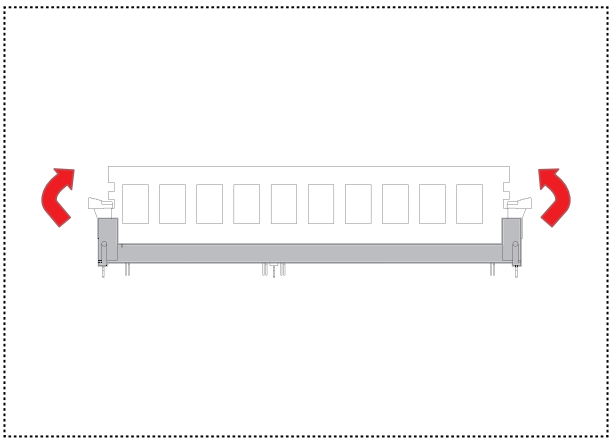
Step 1 Unlock the DIMM socket by pressing the retaining clips outward.



Step 2 Insert the memory module into the slot. Make sure that the DIMM notch is accurately positioned.



Step 3 Close the retaining clips to complete installation.



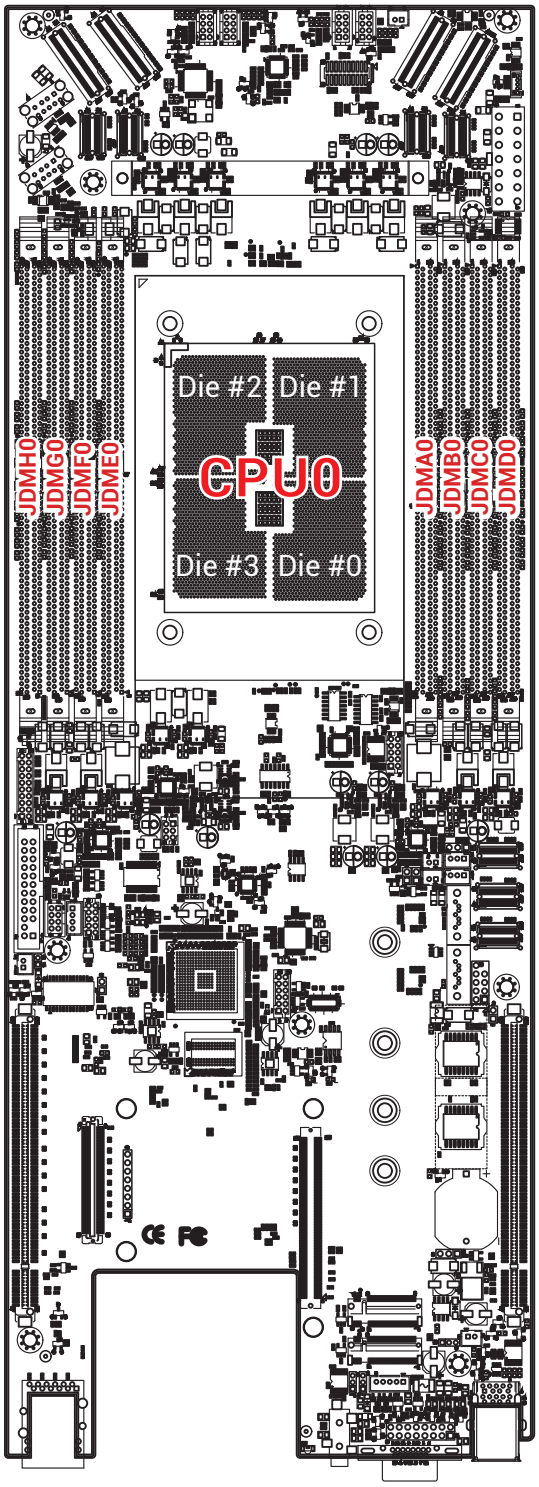
2.2.2 DIMM Placement

The DIMMs are displayed on the Aurigaboard as JDMA0, JDMB0, JDMC0, JDMD0, JDME0, JDMF0, JDMG0, JDMH0 as demonstrated. JDMA0 and JDME0 are the located nearest to the CPU.

To ensure satisfactory performance, you need to:

☑ Verify the DIMM type:
This product supports DDR4 RDIMM/ LRDIMM/NVDIMM-N
with EEC(Error Correction Code).

☑ Verify if all of the DIMMs installed are of the same DIMM type to avoid memory failure and loss of performance speed.



2.2.3 DIMM Slot Installation

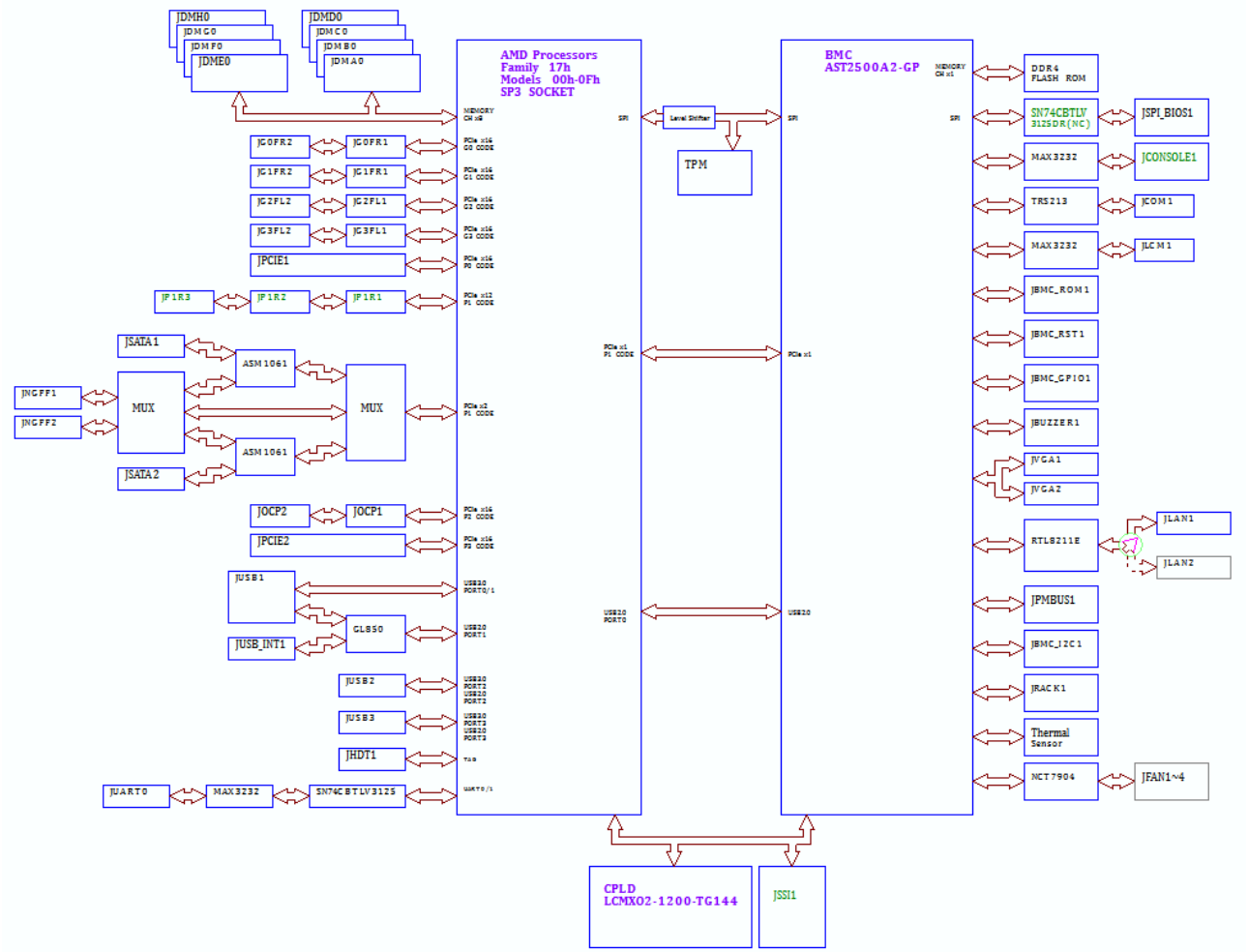
Populate the DIMM slots according to the corresponding Die as suggested to ensure a stable system performance.

Die #0: JDMC0 / JDMD0
Die #1: JDMA0 / JDMB0
Die #2: JDMG0 / JDMH0
Die #3: JDME0 / JDMF0

Chapter 3. Motherboard Settings

This section provides illustrations that display the internal jumpers, connectors, and system LED indicators on the Auriga motherboard. The motherboard layout and essential connectors are listed below for your reference.

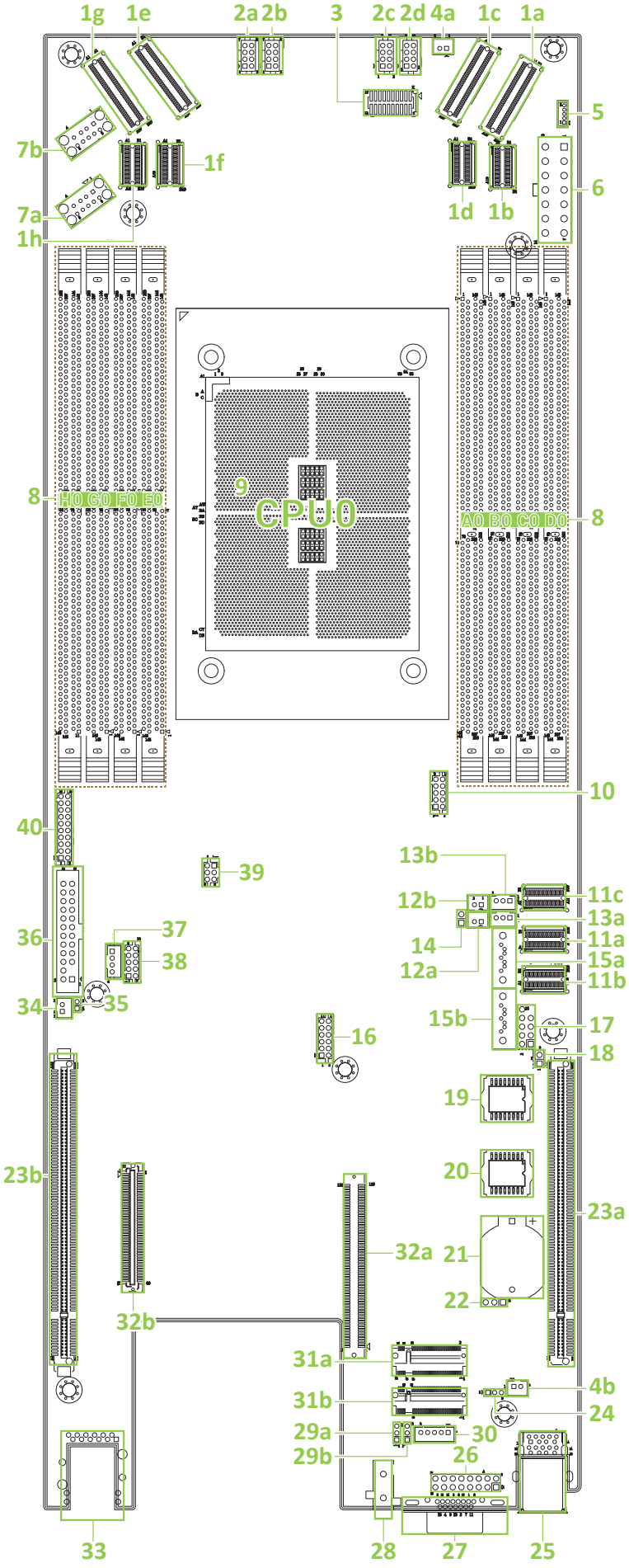
3.1 Block Diagram



3.2 Content List

Connector/Jumper/Header		Placement	Connector/Jumper/Header		Placement
1a 1b 1c 1d 1e 1f 1g 1h	PCIe Bus SAS slimline Connector	JG0FR1 JG0FR2 JG1FR1 JG1FR2 JG2FL1 JG2FL2 JG3FL1 JG3FL2	21	Battery Socket (For CR2032)	JBAT1
2a 2b 2c 2d	Fan Header	JFAN1 JFAN2 JFAN3 JFAN4	22	SOC CMOS Clear Jumper	JCMOS1
3	HDT Connector	JHDT1	23a 23b	Standard PCIe slot x16	JPCIE1 JPCIE2
4a 4b	Remote Thermal Sensor Connector	JTHM1 JTHM2	24	BMC Debug Port Header	JBMC_DP1
5	PMBUS I²C Header	JPMBUS1	25	External USB2.0/3.0 x2 Connector	JUSB1
6	Power Supply Connector	JPWR1	26	Front VGA Header	JVGA2
7a 7b	Internal USB2.0/3.0 Type-A Vertical Connector	JUSB2 JUSB3	27	External VGA Connector	JVGA1
8	DIMM Slot	JDMA0, JDMB0, JDMC0, JDMD0, JDME0, JDMF0, JDMG0, JDMH0	28	BMC Console Port	JCONSOLE1
9	CPU Socket	JCPU0	29a 29b	BMC Console Port Select Header	J3 J4
10	SOC UART Header	JUART0	30	Front Plane Controller Header	JLCM1
11a 11b 11c	PCIe Bus SAS slimline Connector	JP1R1 JP1R2 JP1R3 (Reserve)	31a 31b	NGFF(M.2) Connector	JNGFF1 JNGFF2
12a 12b	SATA DOM Power Jumper	JSATA1_PWR1 JSATA2_PWR1	32a 32b	OCP Connecter	JOCP1 JOCP2
13a 13b	SATA DOM Power Jumper	JSATA1_PWR2 JSATA2_PWR2	33	RJ45 Connector	JLAN1
14	BMC Reset Jumper	JBMC_RST1	34	Chassis Intrusion Header	JINTRUDER1
15a 15b	SATA HDD Connector	JSATA1 JSATA2	35	BMC Buzzer Header	JBUZZER1
16	LPC Debug Port Header	JLPC1	36	SSI Front panel Header	JSSI1
17	Front I/O USB Header	JUSB_INT1	37	IPMB PMBus Header	JBMC_I2C1
18	BMC Enable/Disable Jumper	JBMC_DIS1	38	BMC COM2 Header	JCOM1
19	BMC Firmware ROM Socket	JBMC_ROM1	39	GPIO Header	JBMC_GPIO1
20	System BIOS ROM Socket	JSPI_BIOS1	40	Front panel Header for Rack	JRACK1

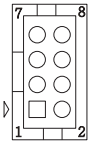
3.3 Connector and Jumper Placement



3.4 Connector and Jumper Definintion

2a Fan Header (JFAN1)

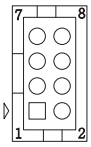
8-pin header that connects fan 1.



FANTACH_2	1	2	FANTACH_1
+12V_S0	3	4	+12V_S0
SYS1_FAN_PWM_C	5	6	SYS1_FAN_PWM_C
GND	7	8	GND

2b Fan Header (JFAN2)

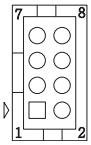
8-pin header that connects fan 2.



FANTACH_4	1	2	FANTACH_3
+12V_S0	3	4	+12V_S0
SYS2_FAN_PWM_C	5	6	SYS2_FAN_PWM_C
GND	7	8	GND

2c Fan Header (JFAN3)

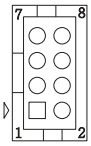
8-pin header that connects fan 3.



FANTACH_6	1	2	FANTACH_5
+12V_S0	3	4	+12V_S0
SYS3_FAN_PWM_C	5	6	SYS3_FAN_PWM_C
GND	7	8	GND

2d Fan Header (JFAN4)

8-pin header that connects fan 4.



FANTACH_8	1	2	FANTACH_7
+12V_S0	3	4	+12V_S0
SYS4_FAN_PWM_C	5	6	SYS4_FAN_PWM_C
GND	7	8	GND

4a Remote Thermal Sensor Connector (JTHM1)

2-pin header employed for monitoring temperature.

1	HM_TD4+
2	HM_TD4-

4b Remote Thermal Sensor Connector (JTHM2)

2-pin header employed for monitoring temperature.

1	HM_TD2+
2	HM_TD2-

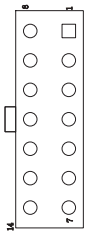
5 PMBUS I²C Header (JPMBUS1)

5-pin header for power management.

1	SMB_PMBUS_CLK
2	SMB_PMBUS_DATA
3	PMBUS_ALERT_N
4	GND
5	+3V3_S5

6 Power Supply Connector (JPWR1)

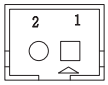
14-pin connector for main power supply.



+12V_S0	8	1	GND
+12V_S0	9	2	GND
+12V_S0	10	3	GND
+12V_S0	11	4	GND
+12V_S0	12	5	GND
+5V_STBY_PSU	13	6	GND
PS_OK_12V	14	7	PS_ON_12V_N

12a SATA-DOM Power Jumper (JSATA1_PWR1)

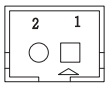
2-pin that supplies power to SATA DOM.



1	+5V_S0_SATA1
2	GND

12b SATA-DOM Power Jumper (JSATA2_PWR1)

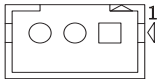
2-pin that supplies power to SATA DOM.



1	+5V_S0_SATA2
2	GND

13a SATA-DOM Power Jumper (JSATA1_PWR2)

3-pin that supplies power to SATA DOM.

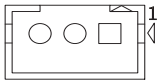


1	GND
2	DOM_PWR1
3	+5V_S0_SATA1

Jumper default Pin-1 & Pin-2

13b SATA-DOM Power Jumper (JSATA2_PWR2)

3-pin that supplies power to SATA DOM.



1	GND
2	DOM_PWR2
3	+5V_S0_SATA2

Jumper default Pin-1 & Pin-2

14 BMC Reset Jumper (JBMC_RST1)

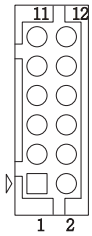
2-pin for resetting BMC jumper.

1	BMC_RESET (BMC SRST#)
2	GND

Jumper default OPEN

16 LPC Debug Port Header (JLPC1)

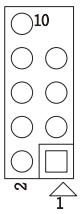
12-pin header for low pin count debug.



LPC_HDR_CLK	2	1	GND
P0_LFRAME_N	4	3	P0_LDRQ0_N
LPC_HDR_RST_N	6	5	P0_SERIRQ
P0_LAD3	8	7	P0_LAD2
+3V3_S0	10	9	P0_LAD1
P0_LAD0	12	11	GND

17 Front I/O USB Header (JUSB_INT1)

9-pin USB header for the front panel.



+5V_HUB2	1	2	+5V_HUB2
USB2_HUB1_DN	3	4	USB2_HUB2_DN
USB2_HUB1_DP	5	6	USB2_HUB2_DP
GND	7-	8	GND
KEY (no pin)	9	10	GND

18 BMC Enable/Disable Jumper (JBMC_DIS1)

2-pin jumper that enables/disables BMC.

1	FW_SPI_CS0_N
2	GND

Jumper default keep OPEN.

22 SOC CMOS Clear Jumper (JCMOS1)

3-pin jumper to reset BIOS setting.

1	+VDDBT_RTC_JP (CR2032)
2	+1V5_RTC (SOC)
3	GND

Jumper default Pin-1 & Pin-2

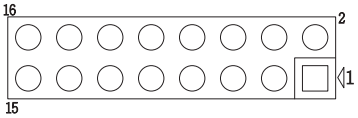
24 BMC Debug Port Header (JBMC_DP1)

3-pin header for BMC debug.

1	RS232_TXD5
2	RS232_RXD5
3	GND

26 Front VGA Header (JVGA2)

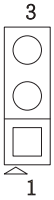
16-pin VGA header for front panel.



DACROA	2	1	GND
NC	4	3	DACGOA
GND	6	5	DDC_DATAO
DACBOA	8	7	GND
AHSYNCO	10	9	NC
DVO_5V	12	11	AVSYNCO
GND	14	13	GND
DDC_CLKO	16	15	GND

29a BMC Console Port Select Header (J3)

3-pin header for selecting BMC console.

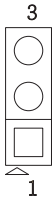


1	TX1
2	PJ_TX
3	TX5

Jumper default Pin-1 & Pin-2

29b BMC Console Port Select Header (J4)

3-pin header for selecting BMC console.

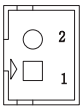


1	RX1
2	PJ_RX
3	RX5

Jumper default Pin-1 & Pin-2

34 Chassis Intrusion Header (JINTRUDER1)

2-pin header for detecting the chassis of being opened.



1	CHASSIS_OPEN_N
2	GND

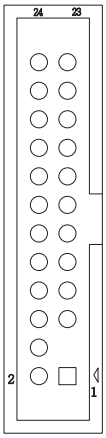
35 BMC Buzzer Header (JBUZZER1)

2-pin internal buzzer/speaker header for BMC.

1	+5V_S0
2	BMC_BUZZER

36 SSI Front panel Header (JSSI1)

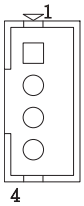
24-pin header for SSI front panel cable.



FP_HDR_PWR_LED	1	2	FP_PWR (+3V3_S5)
KEY (no pin)	3	4	HDR_CHASSIS_ID_LED (+5V_S5)
FP_PWR_LED_L	5	6	ID_LED_OUT_N
HDD_LED_P (+3V3_S5)	7	8	SYS_HEALTH2#
HDD_LED_N	9	10	SYS_HEALTH#
FP_PWR_BTN_N	11	12	LAN1_ACTLED_PWR
GND	13	14	PHY1_LED0_N
SW_COLD_RST_N	15	16	BMC_I2C_08_SDA
GND	17	18	BMC_I2C_08_SCL
BMC_ID_IN_N	19	20	CHASSIS_OPEN
TEMP_SENSOR (NC)	21	22	LAN2_ACTLED_PWR
FP_NMI_BTN_N	23	24	PHY1_LED1_R

37 IPMB PMBus Header (JBMC_I2C1)

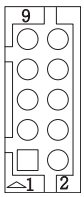
4-pin power management header for BMC.



1	BMC_I2C_01_SDA
2	GND
3	BMC_I2C_01_SCL
4	NC

38 BMC COM2 Header (JCOM1)

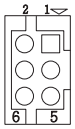
10-pin COM2 header for BMC.



DCDB	2	1	DSRB
RXDB	4	3	RTSB
TXDB	6	5	CTSB
DTRB	8	7	RIB
GND	10	9	NC

39 GPIO Header (JBMC_GPIO1)

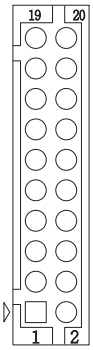
6-pin GPIO BMC header.



RACK_EXTRST_N	2	1	GND
BMC_GPY1	4	3	BMC_I2C_09_SDA
BMC_GPY0	6	5	BMC_I2C_09_SCL

40 Front panel Header for RACK (JRACK1)

20-pin front panel header for rack connection.



RACK_EXTRST_N	1	2	BMC_I2C_08_SCL
GND	3	4	BMC_I2C_08_SDA
BMC_I2C_01_SCL	5	6	GND
BMC_I2C_01_SDA	7	8	RACK_PWM0
GND	9	10	RACK_TACH0
RACK_PMBUS _CLK	11	12	GND
RACK_PMBUS _DATA	13	14	RACK_PWM1
PMBUS_ALERT_N	15	16	RACK_TACH1
RACK_CHASSIS_ OPEN	17	18	RACK_GPIO_EXIN
GND	19	20	CHASSIS_1U2N_N

3.5 System LED Indicator

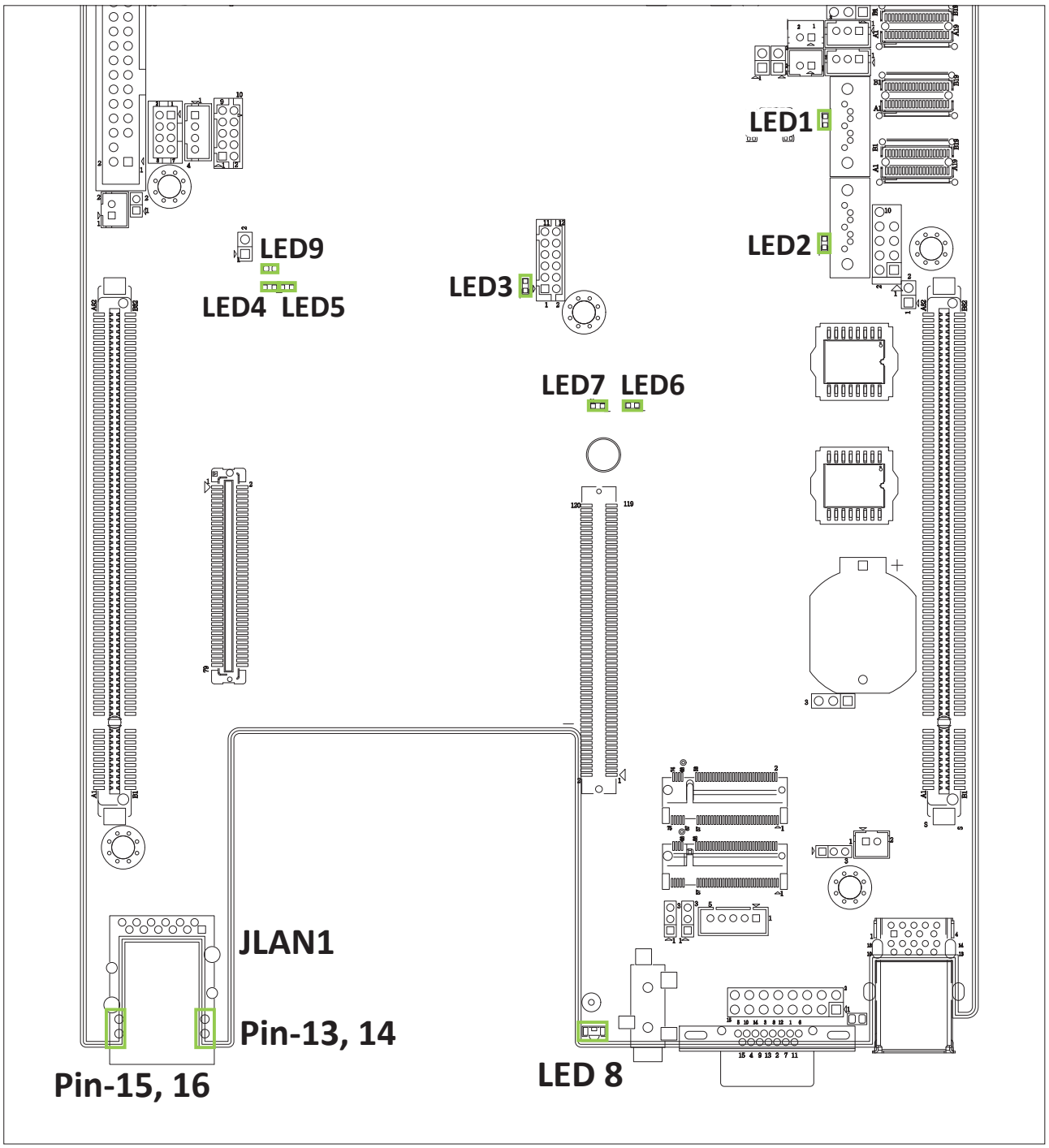
3.5.1 Rear Panel LED

Cable Link/Active Status: LAN1 (Right, JLAN1 Pin-13,14)	Green	1. Cable Plug-In : Green 2. Cable Plug-Out : Off
Linking Speed: LAN1 (Left, JLAN1 Pin-15,16)	Green Amber	1. 1Gbps : Green 2. 100Mbps : Amber 3. 10Mbps & No connect: Off

3.5.2 Internal LED

LED1	JSATA1 status LED (U2005 ASM1061)	On (Blinking)	Indicates SATA is in use when LED is lit.
		Off	Indicates SATA is un-used when LED is dark.
LED2	JSATA2 status LED (U2008 ASM1061)	On (Blinking)	Indicates SATA is in use when LED is lit.
		Off	Indicates SATA is un-used when LED is dark.
LED3	HEART BEAT	On (Blinking)	BMC activity is detected.
		On	BMC is not active.
LED6	RSMRST LED	On	Resume Well Reset is ready.
		Off	Resume Well Reset is not ready.
LED7	POWER GOOD LED	On	System power good is ready.
		Off	System power good is not ready.
LED4, LED9	LAN Speed LED (JLAN1, 15, 16)	On	LAN Linking Speed : (1) 1Gbps : Green (LED9) (2) 100Mbps : Amber (LED4)
		Off	(1) LAN Linking Speed 10Mbps (2) No connection
LED5	LAN status LED (JLAN1,13,14)	On (Blinking)	LAN Cable Linking Status
		Off	LAN* is not active and the LAN cable is not connected.
LED8	UID LED	On (Blinking)	UID activity is detected.
		Off	UID activity is not detected.

3.5.3 Internal LED Indicator Placement



Chapter 4. BIOS Configuration Settings

This chapter demonstrates how to configure the UEFI BIOS settings in your system device. You can enter the BIOS screen during system startup.

To enter BIOS configuration settings,
- Press **Esc** key during the Power-On-Self-Test (POST)

To enter BIOS after POST, you have to restart the system by using one of the three methods:
- Press **Delete** or **Esc**.
- Press the reset button on the system chassis.
- Turn the system off and on.

4.1 Navigation Keys

The navigation keys are listed below.

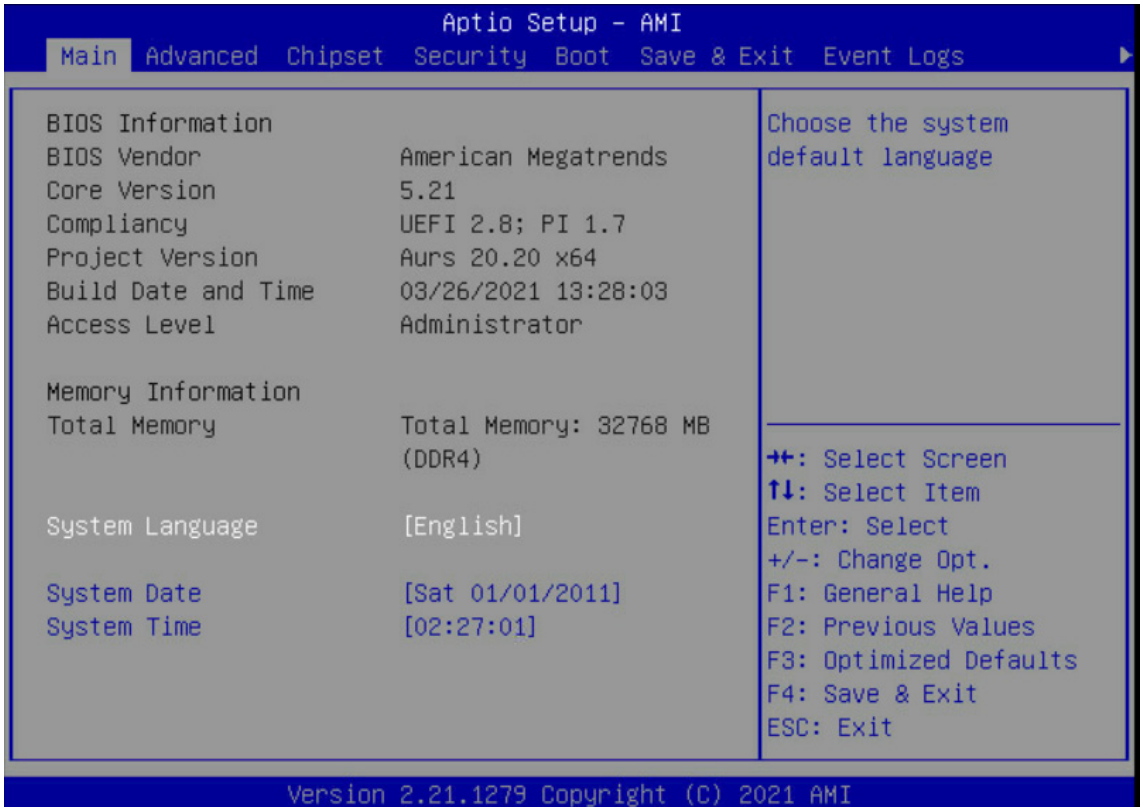
Function Key	Description
< ↑ > < ← > < → > < ↓ >	Select item.
< Enter >	Select and enter sub-screen.
< + > < - >	Modify selected option.
< F1 >	General help.
< F2 >	Previous Value.
< F3 >	Optimized defaults.
< F4 >	Save & Exit.
< F5> < F6 >	Change values.
< F7 >	Discard Change and Exit.
< F9 >	Load Optimal Default for all values.
< F10 >	Save changes and exit.
< F12 >	Print Screen.
< Esc >	Exit the current menu screen.

4.2 Menu

Press ⬅ and ➡ to select the options of the menu bar.
Press **Enter** to access the option screen.

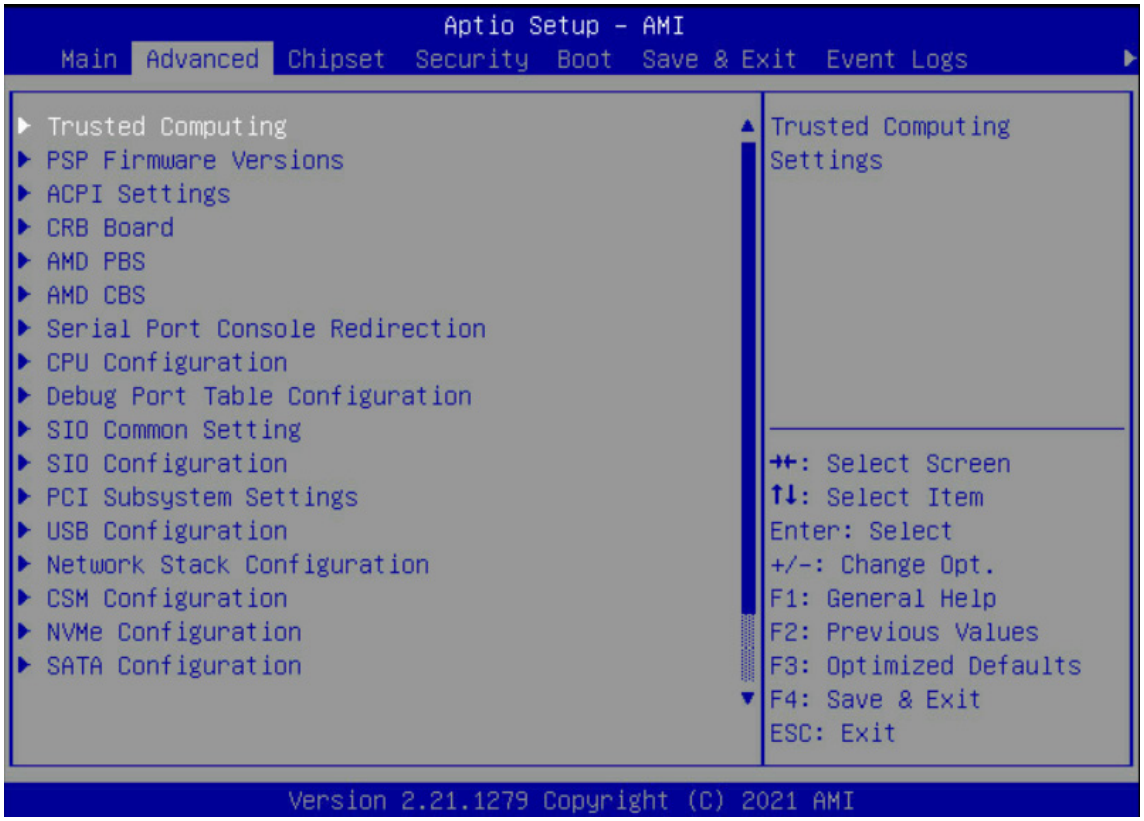
Menu	Description
Main	Displays system information such as CPU bus speed, system memory speed, total installed memory, current EFI language, and system date & time.
Advanced	Allows configuration of advanced system settings such as ACPI features, boot, and chipset configuration.
Chipset	View the configuration of server chipsets.
Security	Sets passwords and security functions.
Boot	Sets boot options such as Quick Boot or USB Boot.
Save and Exit	Save changes and exit, discard changes and exit, discard changes, or load optimal or fail-safe defaults.
Event Logs	Displays the configurations of SMBios Event Logs.
Server Management	Allows configuration of timer, System Event Log, and BMC network.

4.3 Main



Main	
System Language	Configures the language used in the system.
System time	Configures the current time.
System date	Configures the current date.

4.4 Advanced



4.4.1 Trusted Computing

Trusted Computing settings.

Trusted Computing			
Security Device Support	Enables/disables BIOS support for security device.		
	▶Enable	Disable	
SHA-1/256/384 PCR Bank	Enables/disables SHA-1/SHA-256/SHA-384 PCR bank.		
	▶Enable	Disable	
Pending opertation	Schedules an operation for the security deivce. NOTE: Your computer will reboot during restart in order to change the state of the security device.		
	▶None	TPM Clear	
Platform Hierarchy	Enables/disables platform hierarchy.		
	▶Enable	Disable	
Storage Hierarchy	Enables/disables storage hierarchy.		
	▶Enable	Disable	
Endorsement Hierarchy	Enables/disables endorsement hierarchy.		
	▶Enable	Disable	
TPM 2.0 UEFI Spec Version	Select the TCG2 spec version support. • TCG_1_2: The compatible mode for Win8/10. • TCG_2: Support new TCG2 protocol and event format for win10 or later.		
	TCG_1_2	▶TCG_2	
Physical Presence Spec Version	Select to tell O.S. to support PPI spec version 1.2 or 1.3. NOTE: Some HCK tests might not support 1.3.		
	1.2	▶1.3	
Device Select	• TPM 1.2: TPM 1.2 will restrict support to TPM 1.2 devices. • TPM 2.0: TPM 2.0 will restrict support to TPM 2.0 devices. • Auto: Auto will support both with the defualt set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated.		
	▶Auto	TPM 1.2	TPM 2.0

4.4.2 ACPI Settings

System ACPI parameters.

ACI Settings		
Enable ACPI Auto Configuration	Enables/disables BIOS ACPI auto configuration.	
	Enable	►Disable

4.4.3 AMD PBS

AMD PBS setup page.

AMD PBS				
RAS	AMD RAS related settings.			
	RAS Periodic SMI Control	Enables/disables Periodic SMI for polling [MCA Threshold] error.		
		►Enable	Disable	
	SMI Threshold	The [SMI Threshold] limits the number of [MCA Threshold and Deferred Error SMI source] per a Unit time (Defined by [SMI Scale]). (Default: 5 dec interrupts)		
		►5		
	SMI Scale	The [SMI Scale] defines the time scale. (Default: 1000 dec)		
		►1000		
	SMI Scale Unit	The [SMI Scale Unit] defines the unit of time scale. (Default: ms)		
		►millisecond	second	minute
	SMI Period	The [SMI Period] defines the polling interval (Default: 1000 dec, Maximum: 32767 dec, 0: Disable, Unit: ms).		
		►1000		
	GHES Notify Type	Notification type for deferred/corrected errors.		
		►Polled	SCI	
	GHES UnCorr Notify Type	Notification type for uncorrected errors.		
		Polled	►NMI	
	PCIe GHES Notify Type	Notification type for PCIe corrected errors.		
		►Polled	SCI	
	PCIe UnCorr GHES Notify Type	Notification type for PCIe uncorrected errors.		
		Polled	►NMI	
	PCIe Root Port Corr Err Mask Reg	Initialize the PCIe AER Corrected Error Mask register of Root Port.		
		►0		
	PCIe Root Port Un Corr Err Mask Reg	Initialize the PCIe AER Uncorrected Error Mask register of Root Port.		
		►0		
	PCIe Root Port Un Corr Error Sev Reg	Initialize the PCIe AER Uncorrected Error Severity registers of Root Port.		
		►7EF6030		
	PCIe Device Corr Err Mask Reg	Initialize the PCIe AER Corrected Error Mask register of PCIe Device.		
		►0		
	PCIe Device Un Corr Err Mask Reg	Initialize the PCIe AER Uncorrected Error Mask register of PCIe Device.		
		►100000		
	PCIe Device Un Corr Error Sev Reg	Initialize the PCIe AER Uncorrected Error Severity registers of PCIe Device.		
		►7EF6030		
	CCIX GHES Deffered Err Notify Type	Notification type for CCIX deferred error.		
		►Polled	SCI	
	CCIX GHES Corrected Err Notify Type	Notification type for CCIX Corrected error.		
		►Polled	SCI	
	DDR4 DRAM Hard Post Package Repair	This feature allows spare DRAM rows to replace malfunctioning rows via an in-field repair mechanism.		
		Enable	►Disable	

RAS	HEST DMC Structure Support	HEST DMC(Deferred Machine Check) Structure Support	
		Enable	▶Disable
	RAS EINJ Mode	• BIOS: Send APEI EINJ actions to PSP via CPM EINJ SMI callback. • PSP: Send APEI EINJ actions to PSP via PSP Mailbox.	
		BIOS	▶PSP
SPI Locking	Enables/disables SPI Locking for protect ROM part		
	Enable	▶Disable	
iLA Trace Memory En	Reserved 1M bytes MMIO space on 1M boundary when iLA Trace Memory En enabled.		
	Enable	▶Disable	

4.4.4 AMD CBS

AMB CBS setup page.

AMD CBS				
CPU Common Options	Performance	OC Mode	▶Normal Operation	Customized
		SMT Control	Can be used to disable symmetric multithreading. To re-enable SMT, a power cycle is needed after selecting the 'Enable' option. Select 'Auto' base on BIOS PCD (PcdAmdSmtMode) default setting. WARNING: S3 is not supported on systems where SMT is disabled.	
			▶Auto	Enable / Disable
	Prefetcher settings	L1/2 Stream HW Prefetcher	Option to enable/disable L1/L2 Stream HW Prefetcher.	
			▶Auto	Enable / Disable
		L1 Stride Prefetcher	Uses memory access history of individual instructions to fetch additional lines when each access is a constant distance from the previous.	
			▶Auto	Enable / Disable
		L1 Region Prefetcher	Uses memory access history to fetch additional lines when the data access for a given instruction tends to be followed by other data accesses.	
			▶Auto	Enable / Disable
		L2 Up/Down Prefetcher	Uses memory access history to determine whether to fetch the next or previous line for all memory accesses.	
			▶Auto	Enable / Disable
	Core Watchdog	Core Watchdog Timer Enable	Enables/disables CPU watchdog timer.	
			▶Auto	Enable / Disable
	Redirect For Return Dis	From a workaround for GCC/C000005 issue for XV Core on CZ A0, setting MSRC001_1029 Decode Configuration (DE_CFG) bit 14 [DecfgNoRdrctForReturns] to 1.		
		▶Auto	0	1
	Platform First Error Handling	Enables/disables PFEH, cloak individual banks, and mask deferred error interrupts from each bank.		
		▶Auto	Enable	Disable
	Core Performance Boost	Disables CPB.		
		▶Auto	Enable	Disable
	Global C-state Control	Controls IO based C-state generation and DF C-states.		
		▶Auto	Enable	Disable
	Power Supply Idle Control	Power supply idle control.		
		▶Auto	Low Current Idle	Typical Current Idle

CPU Common Options	SEV ASID Count	This fields specifies the maximum valid ASID, which affects the maximum system physical address space. 16TB of physical address space is available for systems that support 253 ASIDs, while 8TB of physical address space is available for systems that support 509 ASIDs.			
		▶Auto	253 ASIDs	509 ASIDs	
	SEV-ES ASID Space Limit Control	▶Auto	Manual		
	Streaming Stores Control	Enables/disbles streaming stores functionality.			
		▶Auto	Enable	Disable	
	Local APIC Mode	▶Auto	xAPIC	x2APIC	
	ACPI _CST C1 Declaration	Determines whether not to declare the state to OS.			
		▶Auto	Enable	Disable	
	MCA error thresh enable	Enables/disables MCA error thresholding.			
		▶Auto	True	False	
	SMU and PSP Debug Mode	When this option is enabled, specific uncorrected errors detected by the PSP or SMU FW will hang and not reset the system.			
		▶Auto	Enable	Disable	
	Xtrig7 Workaround	This workaround is only applicable for Rev A. For Rev A, by default (Auto), the Bronze workaround is applied. Bronze workaround: DbReq and PDM function as expected, breakpoint redirect capability compromised Silver workaround: DbReq, PDM, and breakpoint redirect function as expected, SCAN capability compromised For Rev B, no workaround is applied and changing the selection for this option will not result in any change.			
		▶Auto	No Workaround	Bronze Workaround	Silver Workaround
	PPIN Opt-in	Turns on PPIN feature.			
		▶Auto	Enable	Disable	
	SNP Memory (RMP Table) Coverage	Enable: Entire system memory is covered.			
		▶Auto	Enable	Disable	Custom
	SMEE	Controls secure memory encryption enable.			
		▶Auto	Enable	Disable	
	Action on BIST Failure	Action to take when a CCD BIST failure is detected.			
		▶Auto	Do nothing	Down-CCD	
	Fast Short REP MOVSB	Default is 1, can be set to zero for analysis purposes as long as OS supports it.			
		▶Enable	Disable		
	Enhanced REP MOVSB/STOSB	Default is 1, can be set to zero for analysis purposes as long as OS supports it.			
		▶Enable	Disable		
	REP-MOV/STOS Streaming	Allows REP-MOVS/STOS to use non-caching streaming stores for large sizes.			
		▶Enable	Disable		
	X3D	Override of X3D technology.			
		▶Auto	Disable	1 stack	2 stacks	3 stacks
	IBS hardware workaround	Set if using IBS execution sampling without software workaround for erratum 1,285. May impact performance.			
		▶Auto	Enable		
DF Common Options	Scrubber	DRAM Scrub time	Provides a value that is the number of hours to scrub memory.		
			▶Auto	1 hour	4 hours	8 hours
			Disable	16 hours	24 hours	48 hours
		Poison scrubber control	Control DF: RedirScrubCtrl[RedirScrubMode[1]]		
			▶Auto	Enable	Disable	
		Redirect scrubber control	Control DF: RedirScrubCtrl[RedirScrubMode[0]]		
			▶Auto	Enable	Disable	

DF Common Options	Scrubber	Redirect scrubber limit	Control DF: RedirScrubCtrl[RedirScrubReqLmt]				
			▶Auto	Infinite	2	4	8
	Memory Addressing	NUMA nodes per socket	Specifies the number of desired NUMA nodes per socket. Zero will attempt to interleave the two sockets together.				
			▶Auto	NPS2	NPS4		
		Memory interleaving	Allows for disabling memory interleaving. Note that NUMA nodes per socket will be honored regardless of this setting.				
			▶Auto	Disable			
		Memory interleaving size	Controls the memory interleaving size. The valid values are AUTO, 256 bytes, 512 bytes, 1 Kbytes, 2 Kbytes and 4 Kbytes. This determines the starting address of the interleave (bit 8, 9, 10, 11 or 12).				
			▶Auto	256 Bytes	512 Bytes	1 KB	2 KB
		1TB remap	Attempt to remap DRAM out of the space just below the 1TB boundary. The ability to remap depends on DRAM configuration, NPS, and interleaving selection, and may not always be possible.				
			▶Auto	Do not remap	Attempt to remap		
		DRAM map inversion	Inverting the map will cause the highest memory channels to get assigned the lowest addresses in the system.				
			▶Auto	Enable	Disable		
		Location of private memory regions	Controls whether or not the private memory regions (PSP, SMU and CC6) are at the top of DRAM, at the top of 1st DRAM pair or distributed. Note that distributed requires memory on all dies. Note that it will always be at the top of DRAM if some dies don't have memory regardless of this option's setting.				
			▶Auto	Distributed	Consolidated	Consolidated to 1st DRAM pair	
	ACPI	ACPI SRAT L3 Cache As NUMA Domain	• Enable: Each CCX in the system will be declared as a separate NUMA domain. • Disable: Memory Addressing\NUMA nodes per socket will be declared.				
			▶Auto	Enable	Disable		
		ACPI SLIT Distance Control	Determines how the SLIT distances are declared.				
			▶Auto	Manual			
		ACPI SLIT remote relative distance	Set the remote socket distance for 2P systems as near (2.8) or far (3.2).				
			▶Auto	Near	Far		
	Link	GMI encryption control	Controls GMI link encryption.				
			▶Auto	Enable	Disable		
		xGMI encryption control	Controls xGMI link encryption.				
			▶Auto	Enable	Disable		
		CAKE CRC perf bounds Control	▶Auto	Manual			
		xGMI Link Configuration	Configures the number of xGMI2 links used on a multi-socket system.				
			▶Auto	2 xGMI Links	3 xGMI Links	4 xGMI Links	

DF Common Options	Link	4-link xGMI max speed (Gbps)	▶Auto	6.4	7.467	8.533	9.6		
			10.667	11	12	13	14	15	16	17
			18	19	20	21	22	23	24	25
		3-link xGMI max speed	▶Auto	6.4	7.467	8.533	9.6		
			10.667	11	12	13	14	15	16	17
			18	19	20	21	22	23	24	25
		xGMI TXEQ Mode	Select XGMI TXEQ/RX vetting mode.							
			▶Auto	TXEQ_Lane	TXEQ_Link	TXEQ_RX_Vet				
		xGMI 18GACOFC	xGMI 18GACOFC control.							
			▶Auto	Enable	Disable					
	Disable DF to external IP Sync Flood Propagation	Disables Sync Flood to UMC & downstream slaves.								
		▶Auto	Sync flood enable	Sync flood disable						
	Disable DF sync flood propagation	Control DF: : PIEConfig[DisSyncFloodProp]								
		▶Auto	Sync flood enable	Sync flood disable						
	Frees of DF module	Contols DF: : [DisImmSyncFloodOnFatalError]. Disabling this option sets DF: PIEConfig[DisImmSyncFloodOnFatalError].								
		▶Auto	Enable	Disable						
	CC6 memory region encryption	Controls whether or not the CC6 save/restore memory is encrypted.								
		▶Auto	Enable	Disable						
	System probe filter Memory Clear	Controls whether or not the probe filter is enabled. Has no effect on parts where the probe filter is fuse disable.								
		▶Auto	Enable	Disable						
	Memory Clear	When this feature is disabled, BIOS does not implement MemClear after memory training (only if non-ECC DIMMs are used).								
		▶Auto	Enable	Disable						
	PSP error injection suport	True: Enables error injection.								
		▶True	False							
UMC Common Options	DDR4 Common Options	DRAM timing configuration.								
		DRAM Controller Configuration	DRAM Power Options	Power Down Enable	Enables/ disables DDR power down mode					
					▶Auto					
					Enable					
				Power Down Entry Delay	Specifies value at UMC::CH:: DramTiming17 [19:8] PwrDownDly					
					▶BB8					
				Sub Urg Ref Lower Bound	Specifies the stored refresh limit to required enter sub-urgent refresh mode Constraint: Sub Urg Ref Lower Bound ← Urg Ref Limit. Valid value: 6 ~ 1					
					▶4					

UMC Common Options	DDR4 Common Options	DRAM Controller Configuration	DRAM Power Options	DRAM Maximum Activate Count	Override DIMM SPD Byte 7 [3:0] Maximum Activate Count (MAC) Auto: based on SPD setting.
					►Auto
					200 K
					300 K
					400 K
					500 K
					600 K
					700 K
					Untested MAC
					Unlimited MAC
				DRAM Refresh Rate	►7.8 usec
					3.9 usec
				Self-Refresh Exit Staggering	Tcksrx += (Trfc/n * (UMC_ Number % 4)), here n = 3 or 4 Disabled: does not apply the extra addition.
					Trfc / 3
					Trfc / 4
					►Disable
			Cmd2T	Select between 1T and 2T mode on ADDR/CMD.	
				►Auto	1T / 2T
			Gear Down Mode	►Auto	Enable / Disable
		CAD Bus Configuration	CAD Bus Timin User Controls	Setup time on CAD bus signals to auto or manual.	
				►Auto	Manual
			CAD Bus Drive Strength User Controls	Drive Strength on CAD bus signal to auto or manual.	
				►Auto	Manual
		Data Bus Configuration	Data Bus Configuration User Controls	Specifies the mode for drive strength to auto or manual.	
				►Auto	Manual
		Common RAS	Data Poisoning	Enables/disables data poisoning: UMC_ CH::EccCtrl[UcFatalEn] UMC_ CH::EccCtrl[WrEccEn] Should be enabled/disabled together.	
				►Auto	Enable / Disable
			DRAM Post Package Repair	Enables/disables DRAM Post Package Repair.	
				►Enable	Disable
			RCD Parity	►Auto	Enable / Disable
			DRAM Address Command Parity Retry	UMC_CH::RecCtrl[RecEn][0] and UMC_CH::RecCtrl[MaxParRply]	
				►Auto	Enable / Disable

UMC Common Options	DDR4 Common Options	Common RAS	Disable Memory Error Injection	True: UMC: : CH: : MiscCofg[DisErrInj]=1.		
				▶True	False	
			ECC Configuration	DRAM ECC Symbol Size	DRAM ECC Symbol Size (x4/x8/x16) - UMC_CH: : EccCtrl [EccSymbolSize16, EccSymbolSize]	
					▶Auto	x4
					x8	x16
				DRAM ECC Enable	Use this option to enable/disable DRAM ECC. Auto will set ECC to enable.	
					▶Auto	
					Enable	
					Disable	
				DRAM UECC Retry	Use this option to enable/disable DRAM UECC Retry.	
					▶Auto	
					Enable	
					Disable	
		Security	TSME	Transparent SME: • AddrTweakEn=1 • ForceEncrEn= 1 • DataEncrEn= 0		
				▶Auto	Enable	Disable
			Data Scramble	▶Auto	Enable	Disable
		Phy Configuration	PMU Training	DFE Read Training	Peforms 2D Read Training with DFE on.	
					▶Auto	
					Enable	
					Disable	
				FFE Write Training	Peforms 2D Write Training with FFE on.	
					▶Auto	
					Enable	
					Disable	
				PMU Pattern Bits Control	▶Auto	Manual
	DRAM Memory Mapping	Chip Select Interleaving	Interleave memory blocks across the DRAM chip selects for node 0.			
			▶Auto		Disable	
		Bank Group Swap	Bank Group Swap Alt default: Enabled in BIOS, which has priority than Bank Group Swap. BIOS equation: If Bank Group Swap Alt is enabled, then Bank Group Swap is disabled. Please set Bank Group Swap Alt to Disabled while set Bank Group Swap to Enabled.			
			▶Auto	Enable	Disable	
		Bank Group Swap Alt	▶Auto	Enable	Disable	
		Address Hash Bank 2 ColXor	▶3F8			
		Address Hash Bank	Enables/disables bank address hashing.			
			▶Auto	Enable	Disable	
		Address Hash CS	Enables/disables CS address hashing.			
			▶Auto	Enable	Disable	

UMC Common Options	DRAM Memory Mapping	Address Hash Rm	Enables/disables RM address hashing.			
			▶Auto	Enable	Disable	
		SPD Read Optimization	Enables/disables SPD Read Optimization. • Enabled: SPD reads are skipped for Reserved fields and most of upper 256 Bytes. • Disabled: read all 512 SPD Bytes			
			▶Auto	Enable	Disable	
	NVDIMM	Disable NVDIMM-N Feature	Disables NVDIMM-N feature for memory margin tool.			
			▶No	Yes		
	Memory Bist	MBIST Enable	Enables/disables Memory MBIST.			
			Enable	▶Disable		
		Data Eye	Pattern Select	▶PRBS	SS0	Both
			Pattern Length	This token helps to determine the pattern length. The possible options are N=3~12.		
				▶3		
			Aggressor Channel	This helps read the aggressors channels. If it is enabled, you can read from one or more than one aggressor channel. The default is set to disabled.		
				▶1 Agressor Channel	3 Agressor Channels	
				7 Agressor Channels	Disable	
			Aggressor Static Lane Control	This option, if enabled, will control the Aggressor Static Lane Controls.		
				Enable	▶Disable	
			Target Static Lane Control	Enable	▶Disable	
			Worst Case Margin Granularity	▶Per Chip Select	Per Nibble	
			Read Voltage Sweep Step Size	This option determines the step size for read Data Eye voltage sweep. Supported options are 1, 2 and 4.		
				▶1	2	4
			Read Timing Sweep Step Size	This option supports the step size for read Data Eye. Supported options are 1, 2 and 4.		
				▶1	2	4
			Write Voltage Sweep Step Size	This option determines the step size for write Data Eye voltage sweep. Supported options are 1, 2 and 4.		
				▶1	2	4
			Write Timing Sweep Step	This option supports the step size for write Data Eye. Supported options are 1, 2 and 4.		
				▶1	2	4

UMC Common Options	Memory Bist	Memory Healing BIST	Enables a full memory test. The testing will increase the boot time. BIOS Mem BIST tests the full memory after training. Failing memory will be repaired using soft or hard PPR depending on the PPC configuratoin. The test will take 3 minutes per 16GB of installed memory. Self-Healing BIST runs the JEDEC DRAM self healing if the device supports and DIMM support the feature. The DRAM will do a hard repair for failing memory. The test will take 10 seconds per memory rank per channel. Disable / BIOS Mem BIST / Self-Healing Mem BIST / BIOS and Self-Healing Mem BIST
NBIO Common Options	IOMMU	Enables/disables IOMMU. ▶Auto / Enable / Disable	
	ACS Enable	AER must be enabled for ACS enable to work. ▶Auto / Enable / Disable	
	PCIe ARI Support	Enables Alternative Routing-ID Interpretation. ▶Auto / Enable / Disable	
	PCIe ARI Enumeration	ARI Forwarding Enable for each downstream port. ▶Auto / Enable / Disable	
	PCIe Ten Bit Tag Support	Enables PCIe ten bit tags for supported devices. ▶Auto / Enable / Disable	
	HD Audio Enable	▶Auto / Enable / Disable	
	SMU Common Options	Determinism Control	• Auto: Use the fused Determinism. • Manual: User can set customized Determinism. ▶Auto / Manual
		Fan Control	Fan Table Control • Auto: Use the default fan table. • Manual: User can set customized fan table. ▶Auto / Manual
		cTDP Control	• Auto: Use the fused TDP. • Manual: User can set customized TDP. • TDP is used to define the RC thermal model only. ▶Auto / Manual
		Efficiency Mode En	• 0: use performance optimized CCLK DPM settings. • 1: use power efficiency optimized CCLK DPM settings. ▶Auto / Enable
		Package Power Limit Control	• Auto: Use the fused PPT. • Manual: User can set customized PPT. • PPT will be used as the ASIC power limit. ▶Auto / Manual
		xGMI Link Width Control	• Auto: Use default xGMI link width controller settings. • Manual: User can set custom xGMI link width controller settings. ▶Auto / Manual
		APBDIS	• 0: not APBDIS (mission mode) • 1: APBDIS ▶Auto / 0 / 1
		DF Cstates	• Enable: Enable DF C-states • Disable: Disable DF C-states ▶Auto / Enable / Disable

NBIO Common Options	SMU Common Options	CPPC	FEATURE_CPPC_MASK			
			▶Auto	Enable	Disable	
		HSMP Support	Select HSMP support enable or disable.			
			▶Auto	Enable	Disable	
		DLWM Support	Select DLWM support enable or disable.			
			▶Auto	Enable	Disable	
		Boost Fmax En	• Auto: Use the default Fmax. • Manual: User can set the boost Fmax.			
			▶Auto	Manual		
		EDC Current Tracking	The generation a correctable MCE when the telemetry current value is over the set threshold defined by EDC Current Tracking Current Threshold.			
			Enable	▶Disable		
		LCLK Frequency Control	Root Complex 0x00/0x40/ 0x80/0xC0 LCLK Frequency	Sets Root Complex LCLK Frequency (Bus range 0x00-0x3F). • Auto: Dynamic Frequency Control(Enhanced PIO setting will be in effect). • 593Mhz: Set LCLK Frequency at 593MHz (Overrides Enhanced PIO setting).		
				▶Auto	593Mhz	
		DF Pstate Mode Select	Select the DF PState Mode. • Normal • Limit Highest (FCLK is limited to DF Pstate FCLK Limit, only the highest DF Pstate is used) • Limit All (FCLK is limited to DF Pstate FCLK limit, all DF Pstates are used).			
			▶Auto	Normal	Limit Highest	Limit All
	NBIO RAS Common Options	NBIO RAS Control	0: Disable 1: MCA 2: :Legacy			
			Auto	Disable	MCA	Legacy
		Egress Poison Severity High	Each bit set to 1 enables HIGH severity on the associated IOHC egress port. A bit of 0 indicates LOW severity.			
			▶30011			
		Egress Poison Severity Low	Each bit set to 1 enables HIGH severity on the associated IOHC egress port. A bit of 0 indicates LOW severity.			
			▶4			
		NBIO SyncFlood Generation	This value may be used to mask SyncFlood caused by NBIO RAS options. When set to TRUE SyncFlood from NBIO is masked. When set to FALSE NBIO is capable of generating SyncFlood.			
			▶Auto	Enable	Disable	
		NBIO SyncFlood Reporting	This value may be used to enable SyncFlood reporting to APML. When set to TRUE SyncFlood will be reported to APML. When set to FALSE that reporting well be disabled.			
			▶Auto	Enable	Disable	
		Egress Poison Mask High	These set the enable mask for masking of errors logged in EGRESS_POISON_STATUS. For each bit set to 1, errors are masked. For each bit set to 0, errors trigger response actions.			
			▶FFFCFFFF			

NBIO Common Options	NBIO RAS Common Options	Egress Poison Mask Low	These set the enable mask for masking of errors logged in EGRESS_POISON_STATUS. For each bit set to 1, errors are masked. For each bit set to 0, errors trigger response actions.		
			▶FFFFFFFB		
		Uncorrected Converted to Poison Enable Mask High	These set the enable mask for masking of uncorrectable parity errors on internal arrays. For each bit set to 1, a system fatal error event is triggered for UCP errors on arrays associated with that egress port. For each bit set to 0, errors are masked.		
			▶30000		
		Uncorrected Converted to Poison Enable Mask Low	These set the enable mask for masking of uncorrectable parity errors on internal arrays. For each bit set to 1, a system fatal error event is triggered for UCP errors on arrays associated with that egress port. For each bit set to 0, errors are masked.		
			▶4		
		System Hub Watchdog Timer	This value specifies the timer interval of the SYSHUB Watchdog timer in miliseconds.		
			▶A28		
		SLINK Read Response OK	This value specifies whether SLINK read response errors are converted to an Okay response. When this value is set to TRUE, read response errors are converted to Okay responses with data of all FFs. When set to FALSE read response errors are not converted.		
			▶Enable	Disable	
		SLINK Read Response Error Handling	This value specifies whether SLINK write response errors are converted to an Okay response. When this value is set to 0, write response errors will be logged in the MCA. When set to 1, write response errors will trigger an MCOMMIT error. When this value is set to 2, write response errors are converted to Okay responses.		
			▶Log Errors in MCA	Trigger MCOMMIT Error	Enable
		Log Poison Data from SLINK	This value specifies whether poison data propagated from SLINK will generate a deferred error. When set to TRUE, deferred errors are enabled. When set to FALSE, errors are not generated.		
			Enable	▶Disable	
		PCIe Aer Reporting Mechanism	This value selects the method of reporting AER errors from PCI Express. A value of 1 allows OS First handling of the errors through generation of a system control interrupt (SCI). A value of 2 provides for Firmware First handling of errors through generation of a system management interrupt (SMI).		
			▶Auto	Firmware First	OS First
		Edpc Control	(0) Disabled; (1) Enabled; (3) Auto		
			▶Auto	Enable	Disable
		NBIO Poison Consumption	NBIO Poison Consumption.		
			▶Auto	Enable	Disable

NBIO Common Options	NBIO RAS Common Options	Sync Flood on PCIe Fatal Error	• When 'Sync Flood on PCIe Fatal Error' is True, PcdAmdPcieSyncFloodOnFatal should be set to True. • When 'Sync Flood on PCIe Fatal Error' is False, PcdAmdPcieSyncFloodOnFatal should be set to False. • When 'Sync Flood on PCIe Fatal Error' is Auto, PcdAmdPcieSyncFloodOnFatal should retain its AGESA default.		
			▶Auto	True	False
	Enable AER Cap	Enables Advanced Error Reporting Capability.			
		▶Auto	Enable	Disable	
	Early Link Speed	Sets Early Link Speed.			
		▶Auto	Gen1	Gen2	
	Hot Plug Handling mode	Controls the Hot Plug Handling mode.			
		▶Auto	Firmware First	OS First	
	Presence Detect Select mode	Controls the Presence Detect Select mode.			
		▶Auto	And	Or	
	Preferred IO	Preferred IO Select Type. • Auto: Default			
		▶Auto	Bus		
	Data Link Feature Cap	Data Link feature capability			
		▶Auto	Enable	Disable	
	CV test	Sets this to Enabled to support running PCIECV tool. • Auto: preserve h/w defaults.			
		▶Auto	Enable	Disable	
	SEV-SNP Support	Enable	▶Disable		
FCH Common Options	SATA Configuration Options	SATA Enable	Disables/enables On Chip SATA controller.		
			▶Auto	Enable	Disable
		Sata RAS Support	Disables/enables Sata RAS Support.		
			▶Auto	Enable	Disable
		Sata Disabled AHCI Prefetch Function	Disables/enables Sata Disabled AHCI Prefetch function.		
			▶Auto	Enable	Disable
		Aggresive SATA Device Sleep Port 0/1	▶Auto	Enable	Disable
		SATA Controller Options	SATA Controller Enable	Sata0-7 Enable	Enables/ disables Sata. Each IOD has 4 Sata Controllers.
					▶Auto
					Enable
					Disable
			SATA Controller DevSlp	Socket1 DevSlp	Socket 1 DevSlp0/1 Enable
					▶Auto
					Enable
					Disable

FCH Common Options	SATA Configuration Options	SATA Controller Options	SATA Controller SGPIO	Sata0-7 SGPIO	Enables/ disables SataSgpio on Sata0.
					▶Auto
					Enable
					Disable
	USB Configuration Options	XHCI Controller0/1 enable	Enables/disables USB3 controller.		
			▶Auto	Enable	Disable
		USB ecc SMI Enable	▶Auto	Enable	Off
		MCM USB enable	XHCI2/3 enable (Socket1)	Enables/disables USB3 controller.	
				▶Auto	
				Enable	
				Disable	
	SD Dump Options	SD Configuration Mode	Select SD Mode.		
			SD Dump enable	▶SD Dump disable	
	AC Power Loss Options	Ac Loss Control	Select Ac Loss Control Method.		
			Auto	Previous	Reserved
			Always On	▶Always Off	
	I2C Configuration Options	I2C 0-5 Enable	▶Auto	Enable	Disable
	Uart Configuration Options	Uart 0-3 Enable	▶Auto	Enable	Disable
	FCH RAS Options	ALink RAS Support	▶Auto	Enable	Disable
		Reset after Sync flood	Enables AB to forward downstream sync-flood message to system controller.		
			▶Auto	Enable	Disable
FCH Options	Miscellaneous Options	Boot Timer Enable	Boot timer enable. • Enable: force PMx44 bit 24=1. • Disable: force PMx44 bit 27=0. • Auto: PMx44 bit 27= PcdBootTimerEnable.		
			▶Auto	Enable	Disable
NTB Common Options	Socket-0 P0-3 NTB Enable	Enables NTB on Socket-0 P0-3 Link.			
		▶Auto	Enable		
SoC Miscellaneous Control	ABL Console Out Contron	• Auto: Keeps default behavior. • Enable: Enables console out function for ABL. • Disable: Disables console out function for ABL.			
		▶Auto	Enable	Disable	
Workload Tuning	Workload Profile	Select the profile for different workloads.			
		▶Auto	CPU Intensive	Java Throughput	Java Latency
	Performance Tracing	Enables to allow capturing performance traces.			
		▶Auto	Enable	Disable	

4.4.5 Serial Port Console Redirection

Serial Port Console Redirection.

Serial Port Console Redirection						
Console Redirection	Enables/disables console redirection.					
	▶Enable	Disable				
Console Redirection Settings	Terminal Type	▶ANSI	VT100	VT100+	VT-UTF8	
	Bits per second	Select serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.				
		9600	19200	38400	57600	▶115200
	Data Bits	7	▶8			
	Parity	A parity bit can be sent with the data bits to detect some transmission errors. • Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. • Mark: parity bit is always 1. • Space: Parity bit is always 0. • Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.				
		Even	Odd	Mark	Space	▶None
	Stop Bits	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.				
		▶1	2			
	Flow Control	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.				
		▶None	Hardware RTS/CTS			
	VT-UTF8 Combo Key Support	Enables VT-UTF8 Combination Key Support for ANSI/VT100 terminals.				
		▶Enable	Disable			
	Recorder Mode	With this mode enabled only text will be sent. This is to capture Terminal data.				
		Enable	▶Disable			
	Resolution 100x31	Enables/disables extended terminal resolution.				
		Enable	▶Disable			
	Putty Key Pad	Select Function Key and Key Pad on Putty.				
		▶VT100	LINUX	XTERMR6	SCO	ESCN	VT400
Legacy Console Redirection Settings	Redirection COM Port	Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages.				
		▶COM0	COM1			
	Resolution	On Legacy OS, the Number of Rows and Columns supported redirection.				
		▶80x24	80x25			
	Redirect After POST	When Bootloader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to Always Enable.				
		▶Always Enable	Boot Loader			
Console Redirection EMS	Enables/disables console redirection.					
	Enable	▶Disable				

4.4.6 CPU Configuration

CPU configuration parameters.

CPU Configuration		
SVM Mode	Enables/disables CPU virtualization.	
	▶Enable	Disable

4.4.7 Debug Port Table Configuration

Enables/disables DBGP and DBG2 Tables.

Debug Port Table Configuration		
Debug Port Table	Enables/disables Debug Port Table.	
	Enable	▶Disable

4.4.8 SIO Common Setting

SIO Common setting.

SIO Common Setting		
Lock Legacy Resources	Enables/disables Lock of Legacy Resources.	
	Enable	▶Disable

4.4.9 SIO Configuration

SIO configuration.

SIO Configuration				
[*Active*] Serial Port 1/2/3	Views and sets basic properties of the SIO Logical device. Like IO Base, IRQ Range, DMA Channel and Device Mode.			
	Use This Device	▶Enable	Disable	
	Possible	▶Use Automatic Settings	IO=3F8h; IRQ=4; DMA	IO=3F8H; IRQ=3, 4, 5, 7, 9, 10, 11, 12; DMA;
		IO=2F8h; IRQ=3, 4, 5, 7, 9, 10, 11, 12; DMA;	IO=3E8H; IRQ=3, 4, 5, 7, 9, 10, 11, 12; DMA;	IO=2E8h; IRQ=3, 4, 5, 7, 9, 10, 11, 12; DMA;

4.4.10 PCI Subsystem Settings

PCI Subsystem settings.

PCI Subsystem Settings			
Above 4G Decoding	Globally enables/disables 64 bit capable devices to be decoded in above 4G address Sspace (Only if System supports 64 bit PCI decoding).		
	▶Enable	Disable	
SR-IOV Support	If system has SR-IOV capable PCIe devices, this option enables/disables Single Root IO Virtualization Support.		
	Enable	▶Disable	
BME DMA Mitigation	Re-enable Bus Master Attribute disabled during Pci enumeration for PCI Bridges after SMM Locked.		
	Enable	▶Disable	
Hot-Plug Support	Globally enables/disables Hot-Plug support for the entire system. If system has hot-plug capable slots and this option set to enabled, it provides a setup screen for selecting PCI resource padding for hot-plug.		
	▶Enable	Disable	
Onboard Device [Mass Storage Controller]	Change Onboard PCI device or PCI slot settings.		
	Disable Above 4G Decoding	Disables 64 bit capable Device Resources to be allocated above 4G address space.	
		▶Enable	Disable
	Disable PCI Init	Disables BIOS built-in PCI Express initialization for currently selected and down stream PCI device(s).	
		Enable	▶Disable
	Disable PCIe GEN 2	Disables BIOS built-in PCI Express GEN2 initialization for currently selected and down stream PCI device(s).	
		▶Enable	Disable

4.4.11 USB Configuration

USB configuration parameters.

PCI Subsystem Settings					
Legacy USB Support	Enables Legacy USB support. Auto option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.				
	Auto	▶Enable	Disable		
XHCI Hand-off	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.				
	▶Enable	Disable			
USB Mass Storage Driver Support	Enables/disables USB mass storage driver support.				
	▶Enable	Disable			
Port 60/64 Emulation	Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.				
	▶Enable	Disable			
USB transfer time-out	The time-out value for Control, Bulk, and Interrupt transfers.				
	1 sec	5 sec	10 sec	▶20 sec	
Device reset time-out	USB mass storage device Start Unit command time-out.				
	10 sec	▶20 sec	30 sec	40 sec	
Device power-up delay	Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.				
	▶Auto	Manual			
AMI Virtual CDROM0/1/2/3 1.00	Mass storage device emulation type. 'AUTO' enumerates devices according to their media format. Optical drives are emulated as 'CDROM', drives with no media will be emulated according to a drive type.				
	▶Auto	Floppy	Forced FDD	Hard Disk	CD-ROM
AMI Virtual HDisk0/1/2/3 1.00	Mass storage device emulation type. 'AUTO' enumerates devices according to their media format. Optical drives are emulated as 'CDROM', drives with no media will be emulated according to a drive type.				
	▶Auto	Floppy	Forced FDD	Hard Disk	CD-ROM

4.4.12 Network Stack Configuration

Network Stack setting.

SIO Common Setting		
Network Stack	Enables/disables UEFI Network Stack.	
	Enable	▶Disable

4.4.13 CSM Configuration

Enables/disables Option ROM execution settings.

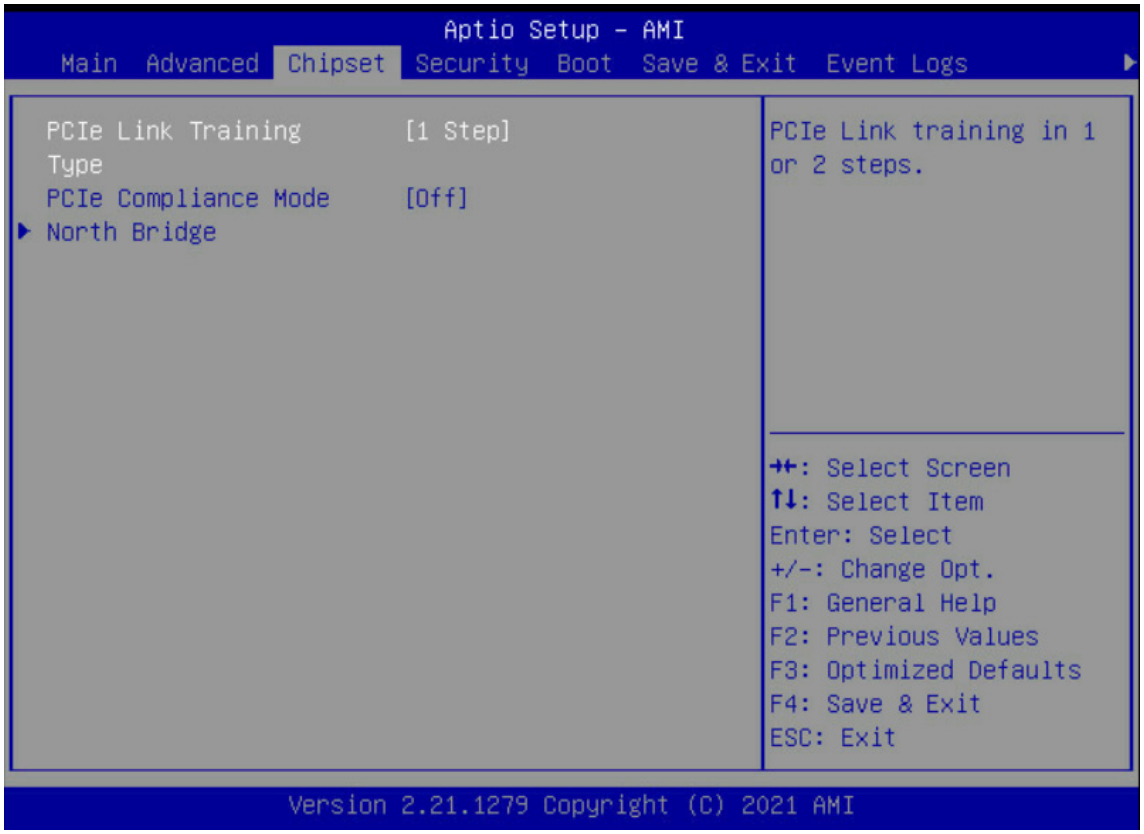
CSM Configuration			
CSM Support	Enables/disables CSM Support.		
	▶Enable	Disable	
GateA20 Active	• Upon Request: GA20 can be disabled using BIOS services. • Always: Do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.		
	▶Upon Request	Always	
INT19 Trap Response	BIOS reaction on INT19 trapping by Option ROM: • Immediate: Execute the trap right away. • Postponed: Execute the trap during legacy boot.		
	▶Immediate	Postponed	
Boot option filter	This option controls Legacy/UEFI ROMs priority.		
	UEFI and Legacy	Legacy only	▶UEFI only
Network	Controls the execution of UEFI and Legacy Network OpROM.		
	▶UEFI	Legacy	Do not launch
Storage	Controls the execution of UEFI and Legacy Storage OpROM.		
	UEFI	▶Legacy	Do not launch
Video	Controls the execution of UEFI and Legacy Video OpROM.		
	▶UEFI	Legacy	Do not launch
Other PCI devices	Determines OpROM execution policy for devices other than Network, Storage, or Video.		
	▶UEFI	Legacy	Do not launch

4.4.14 T1s Auth Configuration

Select T1s Auth Configuration.

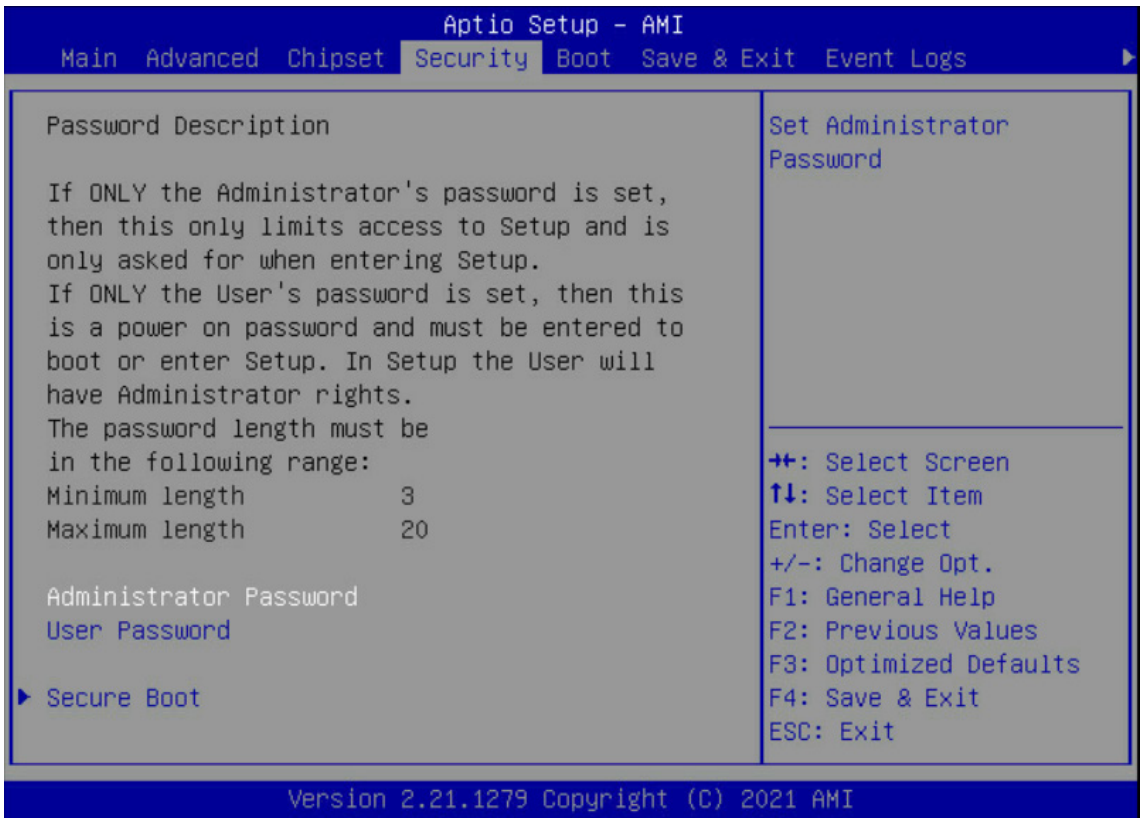
T1s Auth Configuration			
Server CA Configuration	Configures server CA.		
	Enroll Cert	Enroll Cert Using File	Enroll Cert using file.
		Commit Changes and Exit	Commit changes and exit.
		Discard Changes and Exit	Discard changes and exit.
	Delete Cert		

4.5 Chipset



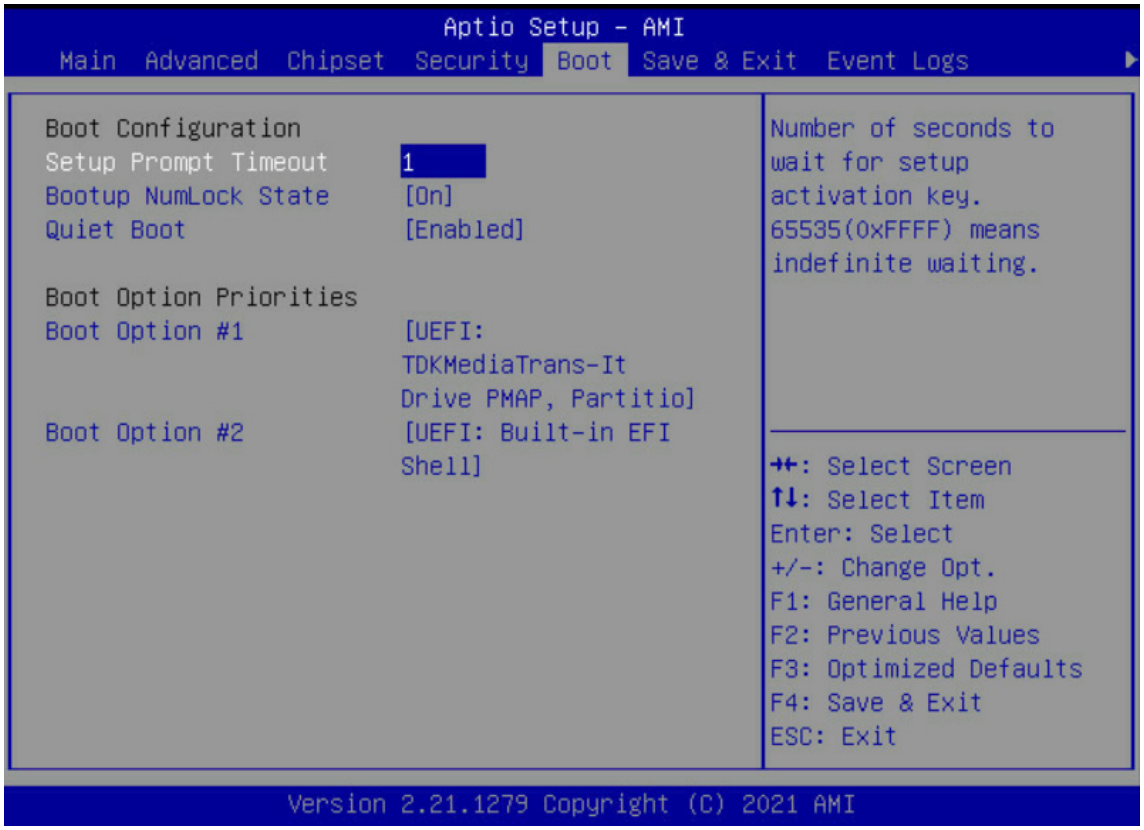
Chipset		
PCIe Link Training	PCIe link training in 1 or 2 steps	
	▶1 step	2 step
PCIe Compliance Mode	PCIe link compliance mode.	
	On	▶Off

4.6 Security



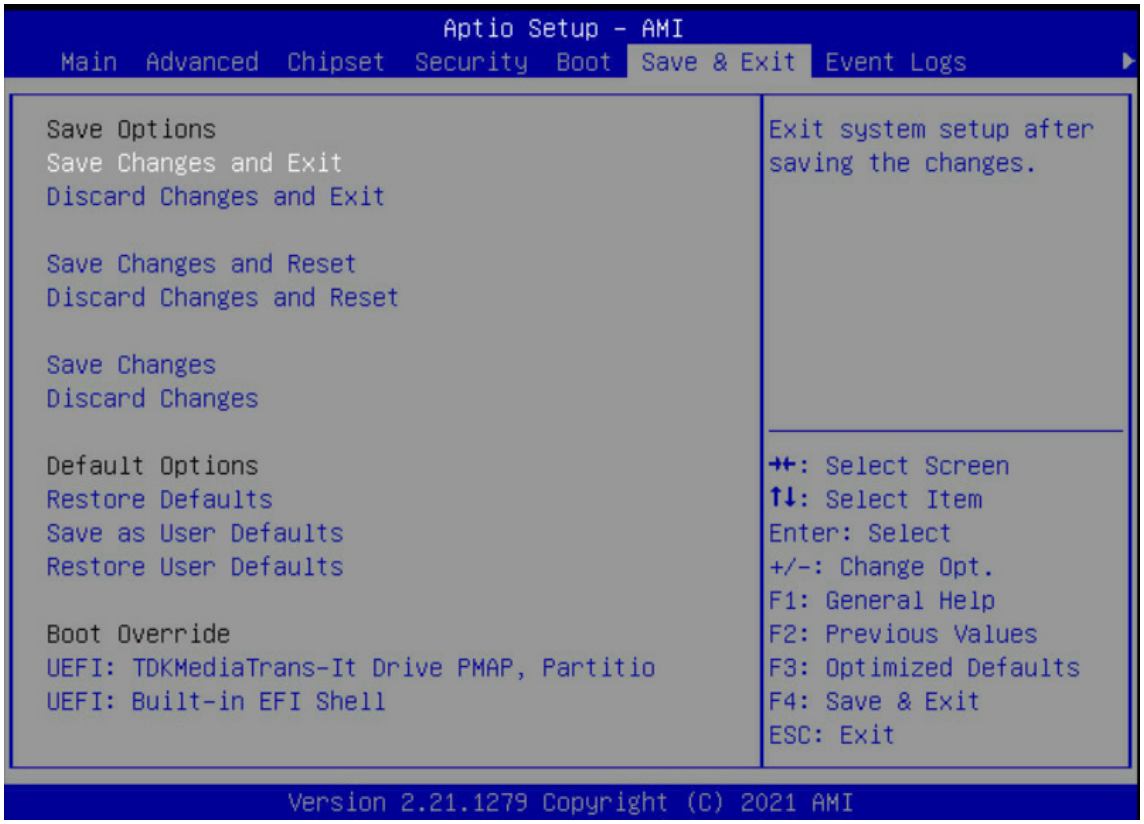
Security			
Administrator Password	Set administer password.		
Set User Password	Create new password.		
Secure Boot	Secure boot configuration.		
	Secure Boot	▶Enable	Disable
	Secure Boot Mode	Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically presen user without full authentication.	
		▶Standard	Custom

4.7 Boot



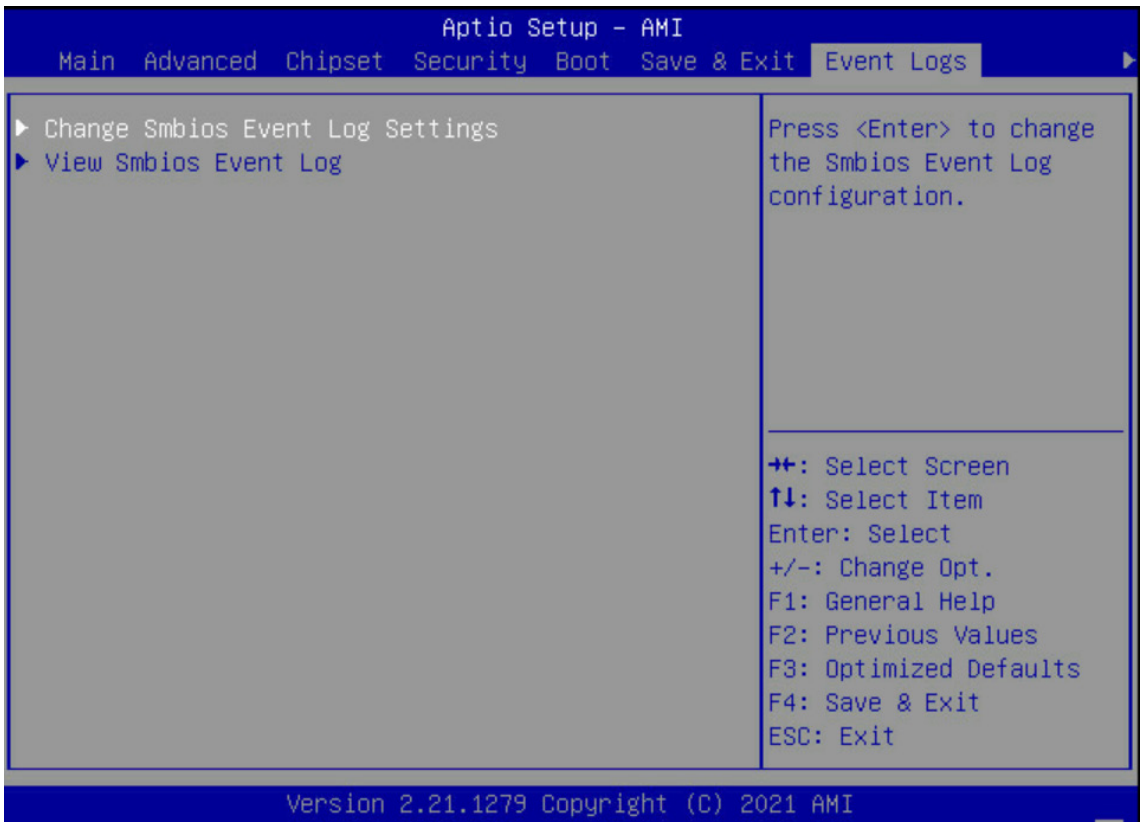
Boot		
Set Prompt Timeout	Number of seconds to wait for setup activation key. 65565 (0xFFFF) means indefinite waiting.	
	▶1	
Bootup Numlock State	Select the keyboard Numlock state.	
	▶On	Off
Quiet Boot	Enables/disables Quiet Boot option.	
	▶Enable	Disable
Boot Option #1/2	Sets the system boot order.	
	▶UEFI: Built-in EFI Shell	Disable

4.8 Save and Exit



Save and Exit	
Save Change and Exit	Exits system setup after saving the changes.
Discard Changes and Exit	Exits system setup without saving any changes.
Save Changes and Reset	Resets the system after saving the changes.
Discard Changes and Reset	Resets system setup without saving any changes.
Save Changes	Saves changes done so far to any of the setup options.
Discard Changes	Discards changes done so far to any of the setup options
Restore Defaults	Restores/loads default values for all the setup options.
Save as User Defaults	Saves the changes done so far as user defaults.
Restore User Ddefaults	Restores the user defaults to all the setup options.

4.9 Event Logs

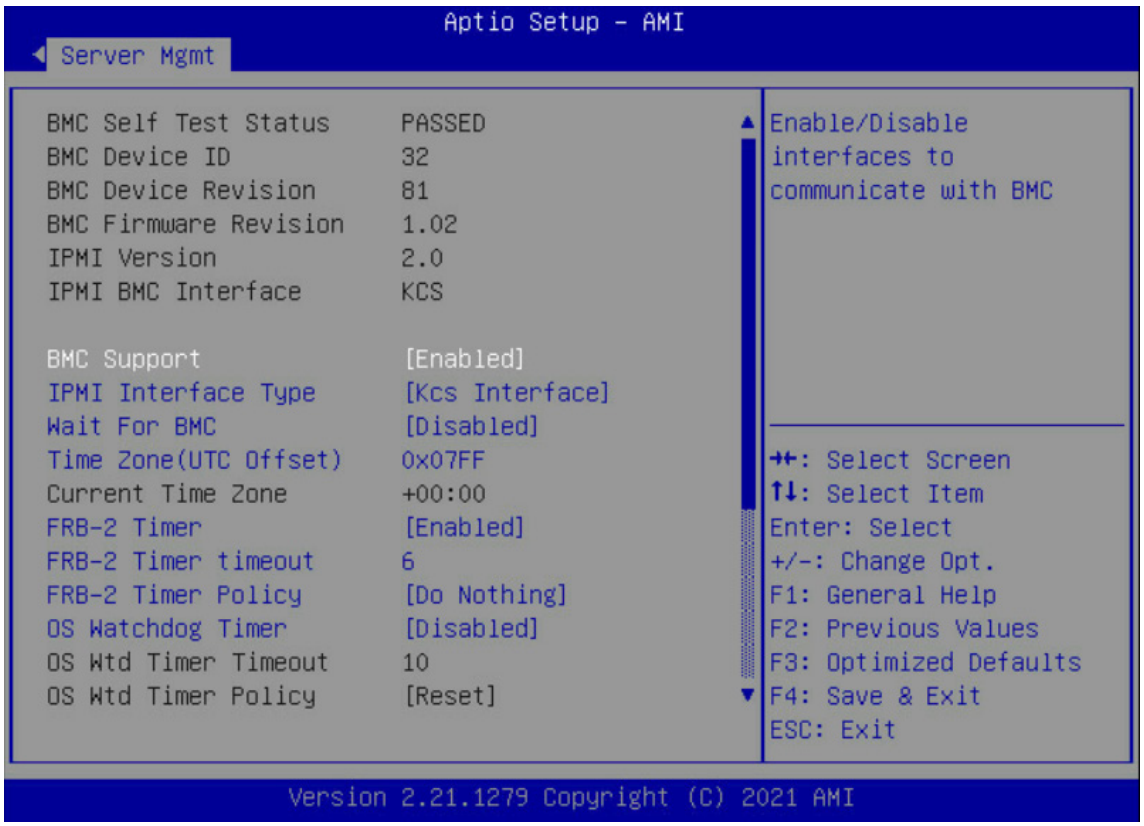


4.9.1 Change Smbios Event Log Settings

Configures Smbios event log.

Boot			
Smbios Event Log	Change this to enable or disable all features of Smbios Event Logging during boot.		
	▶Enable	Disable	
Erase Event Log	Choose options for erasing Smbios Event Log. Erasing is done prior to any logging activation during reset.		
	Yes, Next reset	Yes, Every reset	▶No
When Log is Full	Choose options for reactions to a full Smbios Event Log.		
	Erase Immediately	▶Do Nothing	
Log System Boot Event	Choose option to enable/disable logging of System boot event.		
	▶Enable	Disable	
MECI	Multiple Event Count Increment: The number of occurrences of a duplicate event that must pass before the multiple-event counter of log entry is updated. The value ranges from 0 to 99 minutes.		
	▶1		
METW	Multiple Event Time Window: The number of minutes which must pass between duplicate log entries which utilize a multiple-event counter. The value ranges from 0 to 99 minutes.		
	▶60		
Log EFI Status Code	Enables/disables the logging of EFI status codes as OEM reserved type E0 (if not already converted to legacy).		
	▶Enable	Disable	
Convert EFI Status Codes to Standard Smbios Type	Enables/disables the converting of EFI Status codes to standard Smbios types (not all may be translated).		
	Enable	▶Disable	

4.10 Server Mangement



Server Management				
BMC Support	Enables/disables interfaces to communicte with BMC.			
	▶Enable	Disable		
IPMI Interface Type	Type of Interface to communicate BMC from Host.			
	▶Kcs Interface	Bt Interface		
Wait for BMC	Wait for BMC response for specified time out. In PILOTII, BMC starts at the same time when BIOS starts during AS power ON. It takes around 30 seconds to initialize Host to BMC interfaces.			
	Enable	▶Disable		
Time Zone (UTC Offset)	Enter UTC Offset in hours. i.e. from -24:00 to +24:00. These values will be converted into minutes and programmed to BMC. Enter 0x07FF to consider BIOS time as local time.			
	▶0x07FF			
FRB-2 Timer	Enables/disables FRB-2 timer (POST timer).			
	▶Enable	Disable		
FRB-2 Timer timeouut	Enter value between 1 to 30 minutes for FRB-2 Timer Expiration.			
	▶6	1-30		
FRB-2 Timer Policy	Configures how the system should respond if the FRB-2 Timer expires. Not available is FRB-2 Timer is disabled.			
	▶Do nothing	Reset	Power Down	Power Cycle
OS Watchdog Timer	If enabled, starts a BIOS timer which can only be shut off by Management Software after the OS loads. Helps determine that the OS successfully loaded or follows the OS Boot Watchdog Timer policy.			
	Enable	▶Disable		
Serial Mux	Enables/disables serial Mux configuration.			
	Enable	▶Disable		
System Event Log	SEL Components	Change this to enable/disable event logging for error/progress codes during boot.		
		▶Enable	Disable	
	Erase SEL	Choose options for erasing SEL.		
		Yes, On next reset	Yes, On every reset	▶No

System Event Log	When SEL is Full	Choose options for reactions to a full SEL.			
		Erase Immediately	Delete Oldest Record	▶Do nothing	
	Log EFI Status Codes	Disables the logging of EFI Status codes or log only error code or only progress code or both.			
		▶Error code	Progress code	Both	Disable
Bmc self test log	Logs and report returned by BMC self test command.				
	Erase Log	▶Yes, On every reset		No	
	When log is full	Select the action to be taken when log is full.			
		▶Clear Log		Do not log any more	
BMC network configuration	Configures BMC network parameters.				
	Configuration Address source	Select to configure LAN channel parameters statically or dynamically (by BIOS or BMC). Unspecified option will not modify any BMC network parameters during BIOS.			
		▶Unspecified	Static	Dynamic BMC DHCP	Dynamic BMC Non DHCP
BMC User Settings	Add User	Adds a user.			
	Delete User	Deletes a user.			
	Change User Settings	Changes user settings.			

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