ACBEL POLYTECH INC.

CRPS 2U 1+1 Series

Power Distribution Board Specification

Model Number: R2CU4551A-P00G
R2CU4801A-P00G
R2CU4122A-P00G

AcBel PN: FSK011-000G
FSL025-000G
FSL026-000G

Compatible with R1C series PSU：

※ AC 550W(FSG051), 800W(FSE052), 1200W(FSF050)

※ DC 550W(FSE039), 800W(FSG058)

Revision: A
Release Date: 2020/06/15
Released by: Shan Lin
Change Date:
Changed by:

REVISION LOG

DATE	SECTION	REVISION	ISSUE / DESCRIPTION
2020/06/15		A	Release from S03

1. GENERAL SCOPE

This specification describes the performance characteristic of a DC-DC switching power distribution board (PDB) with a +12V main DC input and a +12Vsb auxiliary input. The PDB will switch into +5V, +3.3V main and +5Vsb auxiliary output and distribute +12V main output. The PDB operates with a single power supply or in 1+1 parallel. Power modules shall support hot-plug and active load share for 12V Main output. Mixed operation of different input type power modules (AC-DC and DC-DC) is allowed.

2. ELETRICAL PERFORMANCE

2.1 POWER BUS AND SIGNAL CONNECTOR

The PDB shall have a common Power Bus and signal connector complying to FCI PCE interconnect series. The exact PN for interconnect is **FCI PN 10035388-102LF (RA) or ALLTOP C21009-102H3-Y or equivalent.**

The Pin definition shall comply with chapter 11.2 and shall provide +12VDC as main input and +12Vsb DC as auxiliary input.

2.2 POWER INPUT SPECIFICATION

2.2.1 Input Voltage/Currents

The maximum input current defines the maximum possible input current to ensure the proper function of the PDB to meet all defined specifications.

INPUT VOLTAGE		INPUT CURRENT	MAX POWER
12VDC	550W	45.83A	550W
	800W	66.67A	800W
	1200W	100A	1200W
$12V_{SB}$ DC		4A	48W

2.2.2 Line dropout *(Refer to Power Module)*

An Input line dropout is a transient condition defined as the line input to the power supply drops to 0 VAC at any phase of the AC line or DC line, for any length of time. During an Input dropout the power supply must meet dynamic voltage regulations requirements. An Input line dropout of any duration shall not cause dripping of the control signals and protection circuits. If the Input dropout lasts longer than the holdup time, the power supply should recover when VIN meets $VIN_{recover}$ and meet all turn on requirements.
An Input dropout of any length shall not cause any damage to the power supply.

Holdup time until Power output goes out of regulations

Loading	Main output	Standby output
80%	12mS	70mS

2.2.3 Efficiency of DC to DC converter

The efficiency of 3.3V and 5V DC to DC converter should meet the efficiency requirements. It's based on without cable no matter input is 230VAC or 115VAC:

Output Voltage	Load	Minimum Efficiency
5V	50%	94%
3.3V	50%	94%

2.2.4 AC Line Transient Specification *(refer to power module)*

AC line transient conditions shall be defined as "sag" and "surge" conditions.

"Sag" conditions are also commonly referred to as "brownout", these conditions will be defined as the AC line voltage dropping below nominal voltage conditions.

"Surge" will be defined to refer to conditions when the AC line voltage rises above nominal voltage.

The power supply shall meet the requirements under the following AC line sag and surge conditions.

AC Line SAG and SURGE transient performance.

AC Line Sag (10sec interval between each sagging)

Duration	Sag	Operating AC voltage	Line frequency	Performance criteria
0 to 1/2 AC cycle	95%	Nominal AC Voltage ranges	50/60Hz	No loss of function or performance
>1 AC cycle	>30%	Nominal AC Voltage ranges	50/60Hz	Loss of function acceptable, self-recoverable
Continues	10%	Nominal AC Voltages	50/60Hz	No loss of function or performance
0 to 1/2 AC cycle	30%	Mid-point of nominal AC Voltages	50/60Hz	No loss of function or performance

2.2.5 Power Recovery

The power supply shall recover automatically (auto recover) after an Input power failure. Input power failure is defined to be any loss of Input power that exceeds the dropout criteria.

2.2.6 Input Line Leakage Current *(Refer to Power module)*

The maximum leakage current to ground for power supply system shall not exceed 3.5mA when tested at 230VAC Input voltages.

2.3 POWER OUTPUT SPECIFICATION

2.3.1 Output Power/Currents

The following table defines the power and current rating of the **R2C** power supply series. The combined output power of all outputs shall not exceed the maximum rated output power, if a combined power rating is specified. The power supply must meet both static and dynamic voltage regulation requirements.

Voltage		Min	Max	Peak
+3.3V		0.1A	18A	20A
+5V		0.1A	24A	28A
+12V	550W	0.5A	45.83A	55A
	800W	0.5A	66.67A	80A
	1200W	0.5A	100A	120A
+5Vsb		0.1A	4A	5.2A

1. Maximum continuous total DC output power should not exceed single PSU max power rating even though in 1+1 parallel condition.
2. Maximum continues combined load on +3.3Vdc and +5Vdc outputs shall not exceed 140W.
3. Maximum peak total DC output power should not exceed 1.2 times of PSU output.

2.3.2 Voltage Regulation

The power supply shall stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise conditions specified in paragraph 2.3.7. All outputs are measured with reference to the return remote sense (ReturnS) signal.

Parameter	MIN	NOM	MAX	Units	Tolerance
+3.3V	+3.13	+3.30	+3.47	V_{rms}	+/-5%
+5V	+4.75	+5.00	+5.25	V_{rms}	+/-5%
+12V	+11.40	+12.00	+12.60	V_{rms}	+/-5%
+5Vsb	+4.75	+5.00	+5.25	V_{rms}	+/-5%

2.3.3 Dynamic Loading

The power supply shall operate within specified limits and meet regulation requirements for step loading and capacitive loading specified below.

The load transient repetition rate shall be tested between 50Hz to 5kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the 1A and the MAX load for main output. The Δ step load may occur anywhere within the Min and the MAX load for standby

Output	△Step Load Size	Load Slew Rate	Capacitive Load
+3.3V	30% of max load	0.5 A/μs	1000 μF
+5V	30% of max load	0.5 A/μs	1000 μF
+12V	60% of max load	0.5 A/μs	2200 μF
+5Vsb	25% of max load	0.5 A/μs	1 μF

2.3.4 Capacitive Loading

The power supply shall meet all requirements with the following capacitive loading ranges.

Output	MIN	MAX	Units
+3.3V	10	12,000	μF
+5V	10	12,000	μF
+5Vsb	1	350	μF
+12V	follow PSU	follow PSU	μF

2.3.5 Maximum Load Change

The power supply shall continue to operate normally when there is a step change ≤ 1 A/μsec between minimum load and maximum load.

2.3.6 Closed loop stability

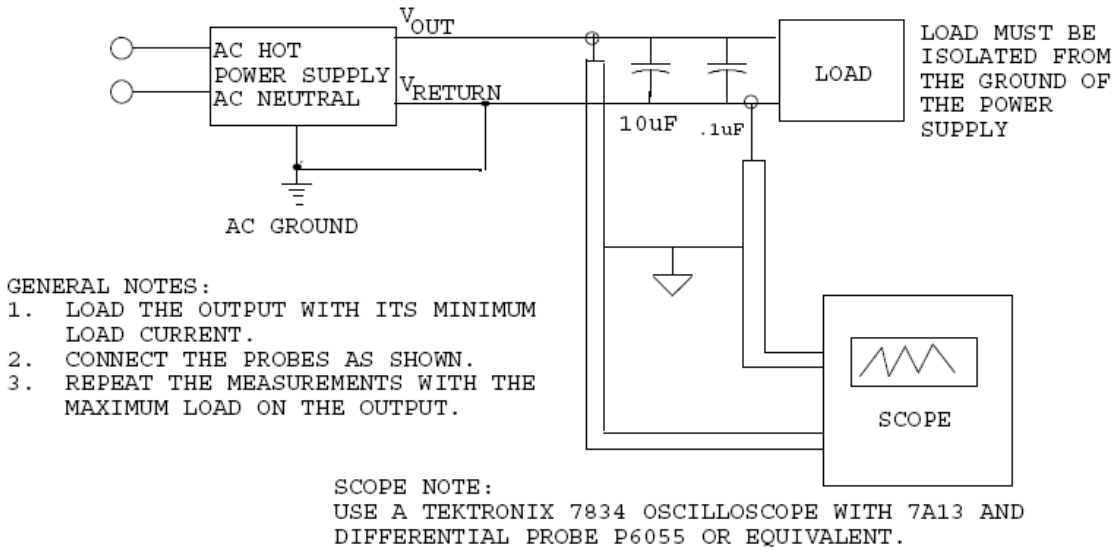
The power supply shall be unconditionally stable under all line/load/transient load conditions including capacitive load ranges specified in Section 2.3.4 and meet a minimum of: 45 degrees phase margin and -6dB-gain margin.

2.3.7 Ripple and Noise

Ripple and Noise shall be measured over a Bandwidth of 20MHz at the power supply output connector. A 0.1μF ceramic capacitor and 10μF of tantalum capacitor shall be placed at each point of measurement.

+3.3V	+5V	+5Vsb	+12V
50 mVp-p	50 mVp-p	50 mVp-p	120 mVp-p

The test set-up shall be as shown below:



3. TIMING REQUIREMENTS

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (Tvout_rise) within 5 to 70ms. For 5Vsb, it is allowed to rise from 1 to 25ms. All main outputs shall rise positive monotonically and have a slop value between 0 V/mS to 0.1V/mS.

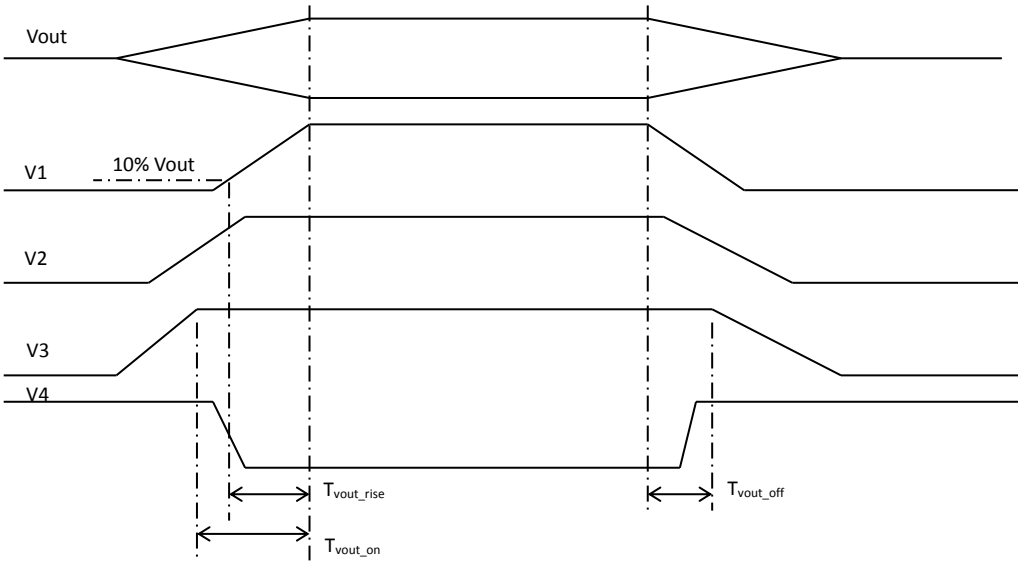
For 5Vsb output any 5ms segment of the 10% to 90% rise time waveform, a straight line draw between the end points of the waveform segment must have s slope ≥ [Vout, nominal /20]V/mS.

Each output voltage shall reach regulation within 50mS (Tvout_on) of each other during turn on of the power supply system. Each output voltage shall fall out of regulation within 400mS (Tvout_off) of each other during turn off.

Table below shows the timing requirements for the power supply being turned on and off via the input power, with PSON held low and the PSON signal, with the input power applied.

Item	Description	MIN	MAX	Units
Tvout rise	Output voltage rise time for all main output	5	70	ms
	Output voltage rise time for the 5Vsb output	1	25	ms
Tvout_on	All main outputs must be within regulation of each other within this time.		50	ms
Tvout_off	All main outputs must leave regulation within this time.		400	ms

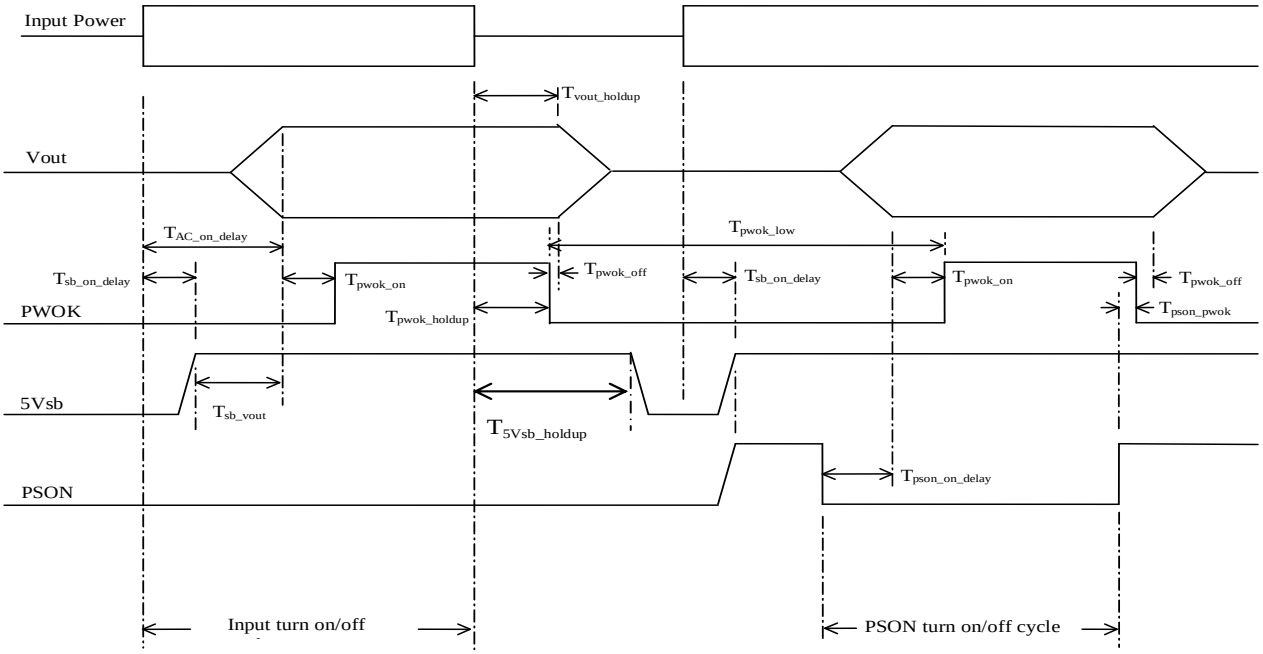
Output Voltage Timing



Turn On/Off Timing

Item	Description	MIN	MAX	UNITS
T sb_on_delay	Delay from ac begin applied to 5Vsb begin within regulation.		1500	ms
T ac_on_delay	Delay from AC begin applied to all output voltage begin within regulation.		2500	ms
T out_holdup	Time all output voltages stay within regulation after loss of AC.	14		ms
T pwok_holdup	Delay from loss of AC to de-assertion of PWOK in single PSU operation mode.	12		ms
T pson_on_delay	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
T pson_pwok	Delay from PSON# de-active to PWOK begin de-asserted.		50	ms
T pwok_on	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	ms
T pwok_off	Delay from PWOK de-asserted to output voltages (3.3V, 5V, 12V) dropping out of regulation limits.	1		ms
T psok_low	Duration of PWOK begin in the de-asserted state during an off/on cycle using AC or the PSON# signal.	100		ms
T sb_vout	Delay from 5Vsb begin in regulation to O/Ps begin in regulation at AC turn on.	50	1000	ms

Turn On/Off Timing (single Power supply)



4. CONTROL AND INDICATOR FUNCTIONS

The following section defines the input and output signals from the power supply. Signals that can be defined as low true use the following convention:
Signal# = low true.

4.1 PSON# INPUT SIGNAL (POWER SUPPLY ENABLE)

The PSON# signal is required to remotely turn on/off the main output of the power supply. PSON# is an active low signal that turns on the main output power rail. When this signal is not pulled low by the system or left open, the outputs (except the Standby output) turn off. PSON# is pulled to a standby voltage by a pull-up resistor internal to the power supply.

PSON# Signal Characteristic

Signal Type	+3.3V TTL Compatible output signal	
PSON# = Low	ON	
PSON# = High or Open	OFF	
	MIN	**MAX**
Logic level low (power supply ON)	0V	1.0V
Logic level high (power supply OFF)	2.0V	3.46V
Source current, V_{pson} = low		1.1mA
Power up delay: $T_{pson\_on\_delay}$	5ms	400ms
PWOK delay: T_{pson_pwok}		50ms
T_{pson} = Delay PSON# disconnect MO OFF		100µsec

4.2 POWER OK (PWOK OR PG) BUS

PWOK is a power good signal and shall be pulled HIGH by the power supply to indicate that all outputs are within regulation limits. When any output voltage falls below regulation limits, an internal failure or when AC power has been removed for a time sufficiently long, so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. The start of the PWOK delay time shall inhibited as long as any power supply output is in current limit.

PWOK / PG Signal Characteristics

Signal Type	+3.3V TTL Compatible output signal	
PWOK = High	Power OK	
PWOK = Low	Power Not OK	
	MIN	**MAX**
Logic level low voltage, I_{sink} = 4mA	0V	1V
Logic level high voltage, I_{source} = 200µA	2.4V	3.46V
Sink current, PWOK = low		4mA
Source current, PWOK = high		2mA
PWOK delay: T_{pwok_on}	100ms	500ms
PWOK rise and fall time		100µsec
Power down delay: T_{pwok_off}	1ms	

4.3 Optional SIGNALS

There're four option signals defined, all signal characteristic be descripted in form as below, those high voltage level should be pulled-up from PDB as 3.3V

option signal	PS_ON = High	PS_ON = Low	Assert during PS_ON = Low	Assert condition	de-assert condition
Alert	H	H	L	anyone PSU assert Alert (please refer to PSU SPEC)	AC cycle or PS_ON/FF cycle
Alarm	L	L	H	PDB fail or anyone PSU fail when 1+1 parallel condition	AC cycle or PS_ON =High
TTL	H	H	L	PDB fail or anyone PSU fail when 1+1 parallel condition	AC cycle or PS_ON =High
Buzzer			Beep	PDB fail or anyone PSU fail when 1+1 parallel condition	AC cycle 、 PS_ON/FF cycle or go back to 1+1 parallel normal condition
Mute	When the buzzer is enabled, this signal is shorted to ground and the buzzer will be disabled.				

5. PROTECTION CIRCUITS

Protection circuits shall cause only the power supply's main outputs to shutdown (latch off). If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15 second or a PSON# cycle HIGH for 1 second must be able to reset the power supply.
The auxiliary output shall not be affected by any protection circuit, unless the auxiliary output itself is affected.

5.1 CURRENT LIMIT

The power supply shall prevent the main and auxiliary outputs from exceeding the values shown in below Table. If the main current limits are exceeded the power supply will shut down and latch off, *the auxiliary output shall be auto recover* ***(Vsb_{AR})*** *after the OCP/SCP had been removed.*

Over Current Protection

Voltage	Over Current Limit (Iout limit)
+3.3V	110% minimum, 150% maximum
+5V	110% minimum, 150% maximum
+5Vsb ***(Auxiliary)AR***	110% minimum, 150% maximum

5.2 OVER VOLTAGE PROTECTION

The power supply shall shutdown and latch off after an over voltage condition occurs. This latch will be cleared by toggling the PSON# signal or by an AC power interruption.

Over Voltage Limits

Output Voltage	MIN (V)	MAX (V)
+3.3V	3.6	4.6
+5V	5.5	6.6
+12V	follow PSU	follow PSU
+5Vsb ***(Auxiliary)AR***	5.5	6.6

5.3 OVER TEMPERATURE PROTECTION

The PDB shall have thermal sensors to measure the internal environmental (T_{env}). The thermal sensors shall be part of a protection circuit to protect against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In a critical over temperature condition, specified in below table, the power system shall be shutdown with the exception of the ***auxiliary output (Vsb_{AR})***.
The Thermal CLST shall be part of the ***OTP_{AR}***.
The PDB will auto recover the power system from this condition, when the temperature is dropping within specification again.

Condition	Warning in °C	Critical in°C	Timing for SMBAlert#/LED
T_{env}	60	65	follow PSU

$T_{env:}$ PDB internal Environment Temperature

6. POWER SUPPLY MANAGEMENT

6.1 I^2C Bus Noise Requirement

The power supplies I^2C Bus' SDA and SCL line shall be clean from noise, which might affect the proper function when utilized with other devices.
The maximum allowed line noise on SDA or SCL is 400mV.

6.2 Address Command

It shall be located at the address set by the A0 and A1 pins.
The PDB Addressing can be changed by utilizing the MFR_CONFIG_ADDRESS command.

PDB position and PSMC address	PM1 B0h/B1h	PM2 B2h/B3h
Pin A0/A1	0/0	1/0

7. ENVIRONMENTAL

7.1 TEMPERATURE REQUIREMENTS

The power supply shall operate within all specified limits over the Top temperature range. The average air temperature difference ($\triangle T_{ps}$) from the inlet to the outlet of the power supply shall not exceed the values shown below Table. All airflow shall pass through the power supply and not over the exterior surfaces of the power supply

ITEM	DESCRIPTION	MIN	MAX	UNITS
Top	Operating temperature range.	0	50	°C
Tnon-op	Non-operating temperature range.	-40	70	°C

7.2 HUMIDITY

Operating: 20% to 85% relative humidity, non-condensing.

Storage: 10% to 90% relative humidity, non-condensing.

7.3 ALTITUDE

Operating: meet up to new CCC 5,000m requirement.

7.4 VIBRATION

Operating: 0.01G2/Hz at 10Hz, 0.02G2/Hz at 20Hz.

Non-Operating: 0.02G2/Hz form 20Hz to 1000Hz.

7.5 MECHANICAL SHOCK

Operating: 5G, no malfunction.

Non-operating: 50G, no damage. Trapezoidal Wave, Velocity change = 4.3m/sec. Three drops in each of six directions are applied to each of the samples.

7.6 EMI/EMC REQUIREMENTS

The power supply shall comply with FCC part 15, CRISP 22 and EN55-22; Class A for both conducted and radiated emissions. Test shall be conducted using a shielded DC output cable to a shielded load. The load shall be adjusted to 100% load. Tests will be performed full load on each output power at 120VAC, 60Hz, and 230VAC, 50Hz.

8. REGULATORY REQUIREMENTS

8.1 MAXIMUM LEAKAGE CURRENT TO GROUND

Less than 3.5mA for entire power system at 230VAC/50Hz

8.2 ELECTROSTATIC DISCHARGE

The objective of ESD test is to determine the susceptibility and immunity of products to electrostatic discharge to which the products may be exposed, when operating under all potential environmental conditions. The test conditions and setup shall conform to that outlined in CISPR24-2 and IEC 801-2 (EN55101-2).

Air discharge: 8KV not allow error.

Contact discharge: 4KV not allow error.

Note: The above test discharge time is 1 time/sec and repeats each test 10 times.

9. RELIABILITY

The MTBF of the power supply can be calculated with the Part-Stress Analysis method of Bell Core SR-332 Issue 1 using the quality factors. A calculated MTBF of the power supply shall be at least 100,000 hours at 40°C ambient with 115VAC and in full load condition.

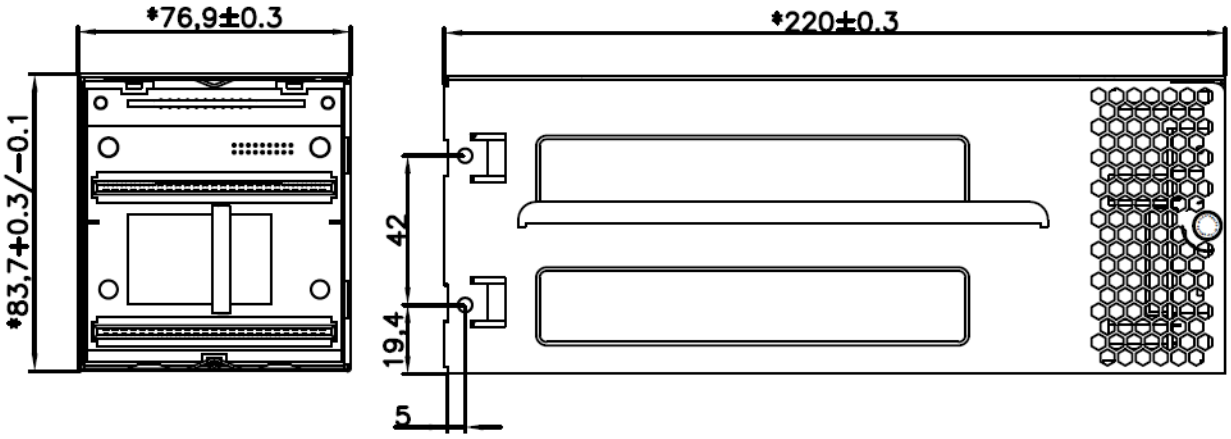
10. RoHS COMPLIANCE

The directive 2002/95/EC of the European Parliament and of the Council of the 27th January 2003, on the restriction of the use of certain hazardous substances in electrical and electronic equipment, requires the reduction of the substances Lead, Mercury, Cadmium, Hexavalent Chromium, Polybrominated Biphenyls (PBB), and Polybrominated Biphenyl ethers (PBDE) in electronic products by July 1, 2006. Unless otherwise noted, all materials used will be compliant with this directive and any subsequent revisions or amendments.

11.MECHANICAL DIMENSIONS

11.1 POWER DISTRIBUTION CAGE DIMENSIONS

Dimension (L x W x H): 220 x 76.9 x 84mm / 10.43 x 3.03 x 3.31inch



Note: Above drawing for reference only, detail drawing refer to mechanical drawing

11.2 DC Output connector

The power supply shall use a card edge output connection for power and signal that is compatible with a 2x25 Power Card Edge connector

Gold finger pin assignment

OUTPUT PIN ASSIGNMENT

PIN	SIGNAL_NAME	PIN	SIGNAL_NAME
A1	GND	B1	GND
A2	GND	B2	GND
A3	GND	B3	GND
A4	GND	B4	GND
A5	GND	B5	GND
A6	GND	B6	GND
A7	GND	B7	GND
A8	GND	B8	GND
A9	GND	B9	GND
A10	+12V	B10	+12V
A11	+12V	B11	+12V
A12	+12V	B12	+12V
A13	+12V	B13	+12V
A14	+12V	B14	+12V
A15	+12V	B15	+12V
A16	+12V	B16	+12V
A17	+12V	B17	+12V
A18	+12V	B18	+12V
A19	PMBus SDA	B19	A0 (SMBus address)
A20	PMBus SCL	B20	A1 (SMBus address)
A21	PSON#	B21	12VSB
A22	SMB Alert#	B22	CR_BUS
A23	Return Sense	B23	12V load share Bus
A24	+12V Remote Sense	B24	Present#
A25	PWOK	B25	NC

11.3 BRACKET OPTIONS

Per customer requirements.